



IP Cores for FPGAs



Aliathon Confidential

Why Aliathon..?

- Highly Skilled Team
- 20 Years+ Telecoms Experience
- Blue-Chip Customers
- FPGA Experts
- Large SoC Design Experience
- World Class Design Environment
- Ongoing Academic Research program



Why Aliathon IP..?

- Designed specifically for FPGAs
 - Resource Efficient
 - High Speed
- Maximum Flexibility
 - Choose from multiple or single functions
 - e.g. Support ALL TU mappings or just one
 - Optimum resource efficiency



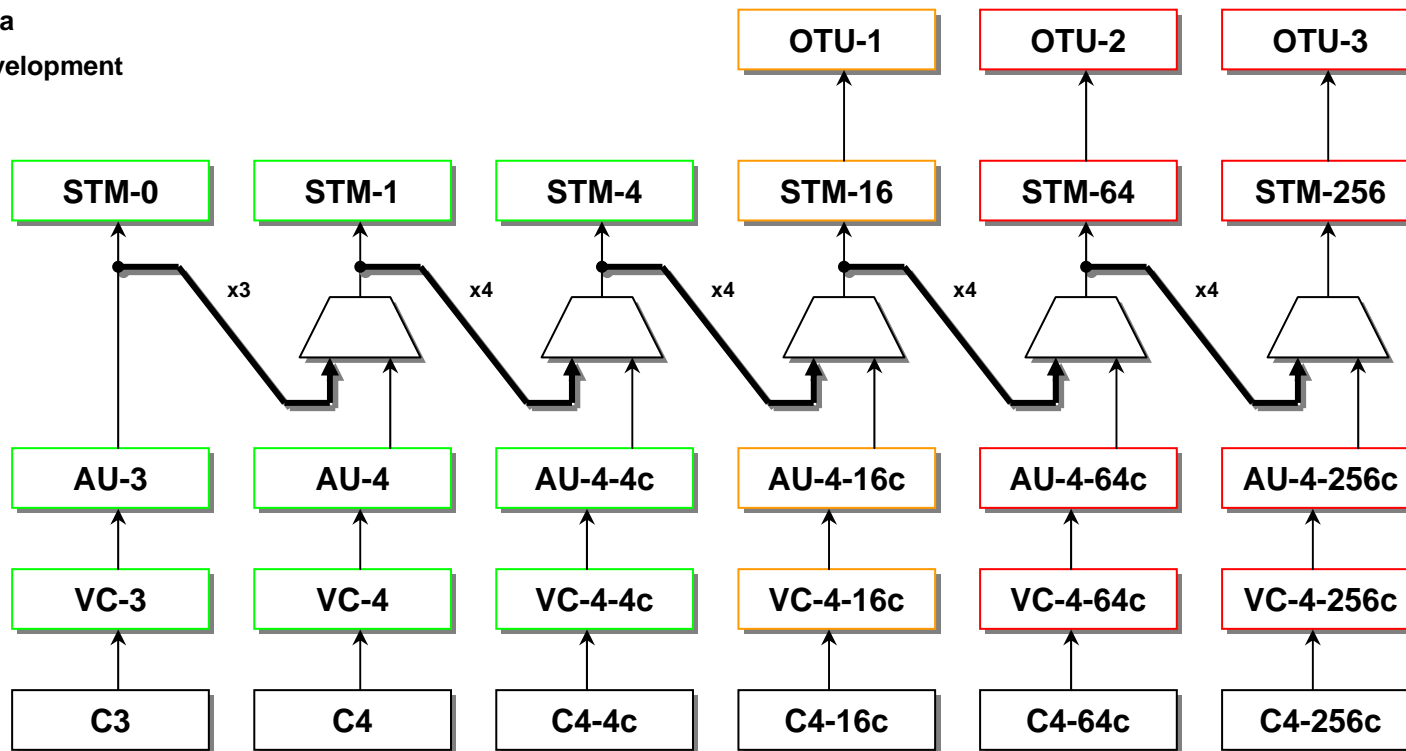
Why Aliathon IP..?

- Complete Solution (System-on-Chip)
 - Reduce Cost
 - Reduce Power
 - Reduce Size and Complexity
- Ease of Upgrade
 - Keep up to date with latest Standards
- Customised Solutions
 - Tailor our Flexible IP to your specific needs



Optical Interface IP

- Mature
- Beta
- Development

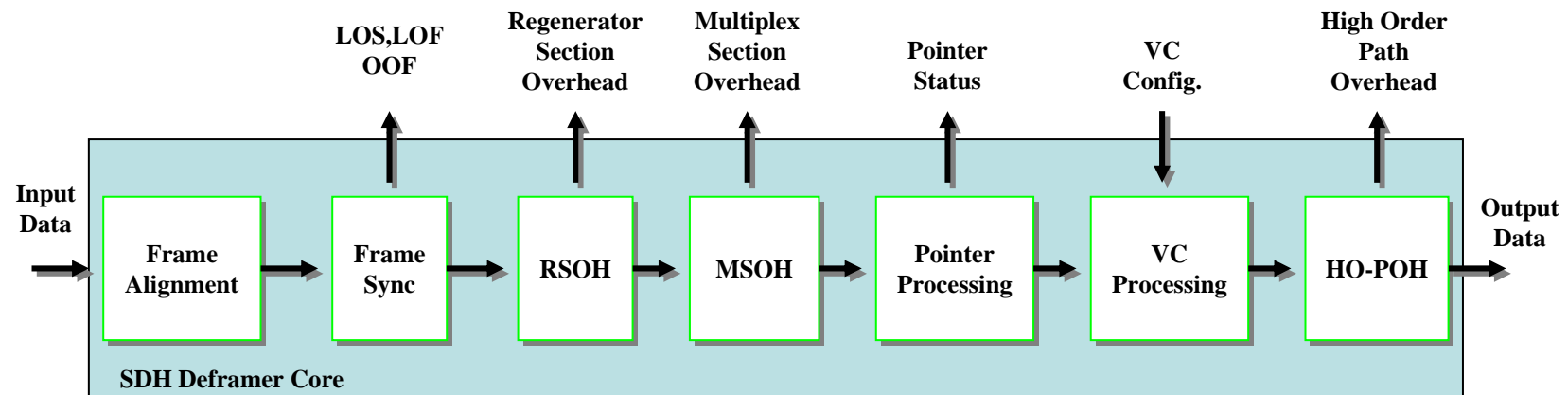


SONET/SDH Deframer STM0-4/OC1-12

- Supports all SONET equivalents of SDH functionality
- Detects SDH frames for STM0/1/4
 - The core may be dynamically switched between rates
- Generates LOS, OOF and LOF alarms
- Descrambles the SDH frames
- Extracts Regenerator Section Overhead and detects B1 errors
- Extracts Multiplex Section Overhead and detects B2 errors
- Processes all AU pointers (up to 12 for VC3 over STM4)
- Extracts VC3, VC4 and VC4-4c, channelised and single-channel
 - All legal combinations of VCs are supported
 - VC settings may be dynamically reconfigured on a per VC basis
- Detects B3 errors for all VCs
- Extracts Higher Order Path Overhead



SONET/SDH Deframer STM0-4/OC1-12

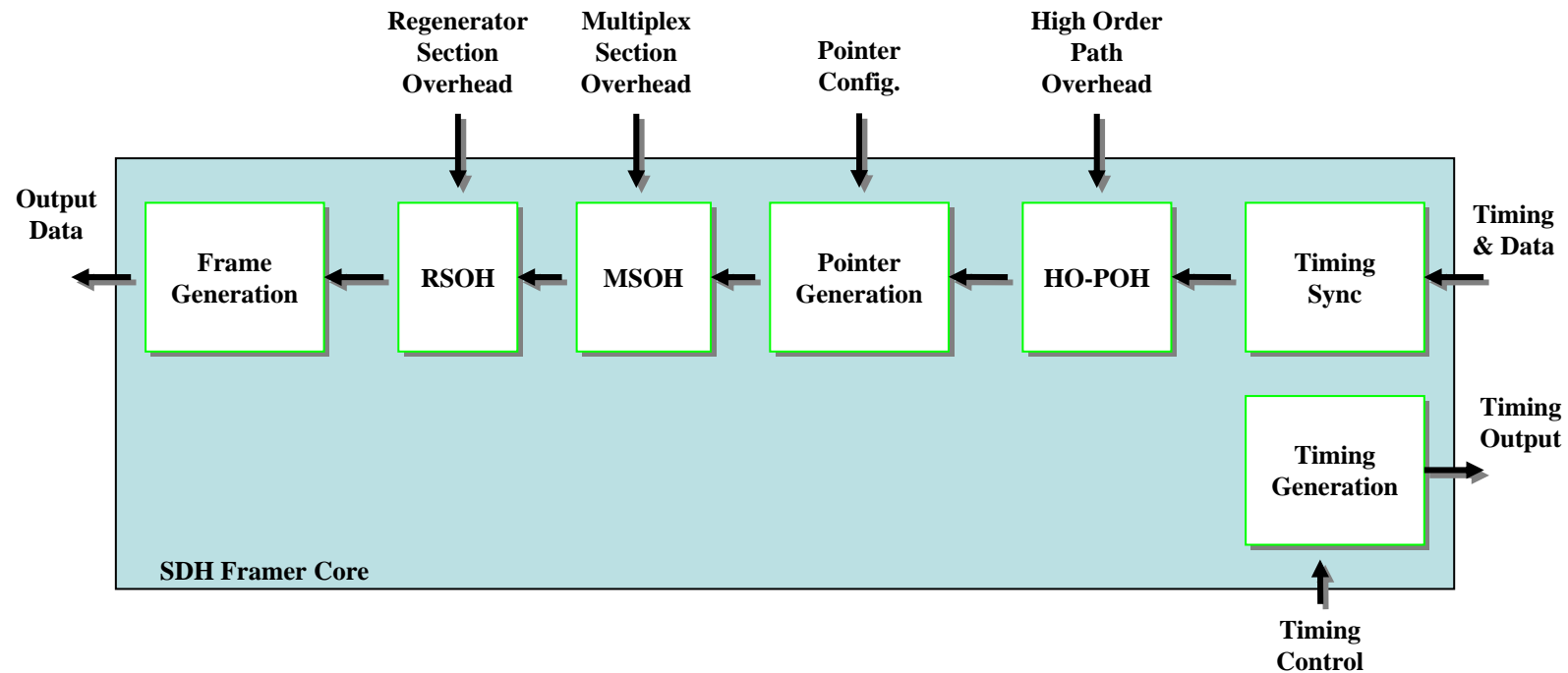


SONET/SDH Framer STM0-4/OC1-12

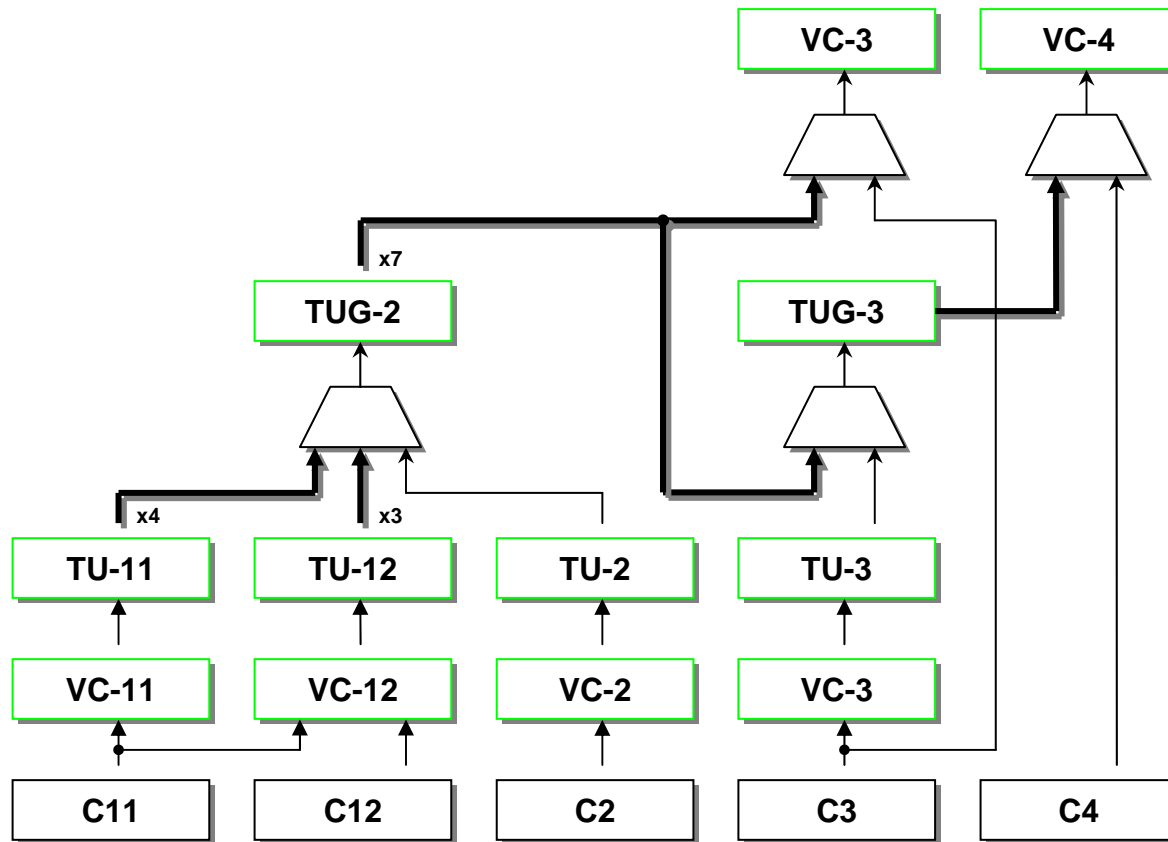
- Supports all SONET equivalents of SDH functionality
- Generates SDH frames for STM0/1/4
 - The core may be dynamically switched between SDH rates
- Scrambles the SDH frames
- Inserts Regenerator Section Overhead and calculates B1 values
- Inserts Multiplex Section Overhead and calculates B2 values
- Generates all AU pointers (up to 12 for VC3 over STM4)
- Inserts VC3, VC4 and VC4-4c, channelised and single-channel
 - All legal combinations of VCs are supported
 - VC settings may be dynamically reconfigured on a per VC basis
- Generates B3 values for all VCs
- Inserts Higher Order Path Overhead



SONET/SDH Framer STM0-4/OC1-12



Optical Mapping IP

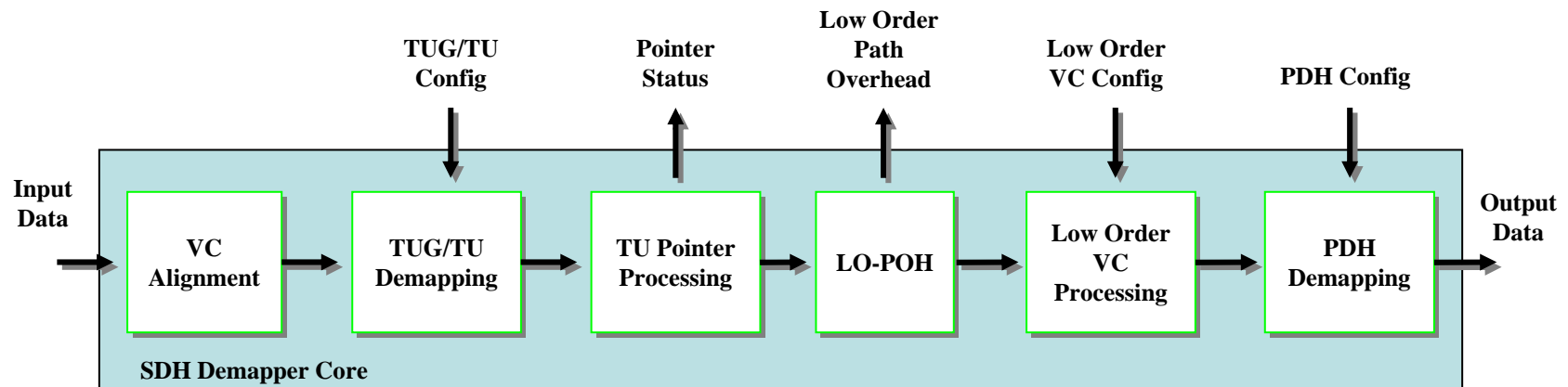


SONET/SDH Demapper STM0-4/OC1-12

- Accepts up to 12 input VCs
 - VCs can be a mix of VC3, VC4, and VC4-4c
- Demaps TUG3 from VC4 and TUG2 from VC3 or TUG3
- Demaps TUs (TU11, TU12 and TU2) from TUG2
 - TU type can be dynamically configured on a per TUG2 basis
 - TU3 within TUG3 is also supported, as is VC11 over TU12
- Processes all TU pointers
 - Including the TU3 pointer for TU3 over TUG3
- Extracts all Lower-Order Path Overhead
- Verifies BIP-2 calculations (B3 in the case of TU3 over TUG3)
- Demaps PDH from VC and TU payloads
 - All mappings for TU11, TU12, TU2, VC3 and VC4 are supported
 - Demapping type may be dynamically configured on a per-TU/VC basis
- Provides a multi-channel output of up to 336 TUs (TU11 over STM4)
- Plugs directly into SDH Deframer core for a complete SDH solution
 - Also into PDH Deframer cores (E1/T1 and E3/T3)



SONET/SDH Demapper STM0-4/OC1-12

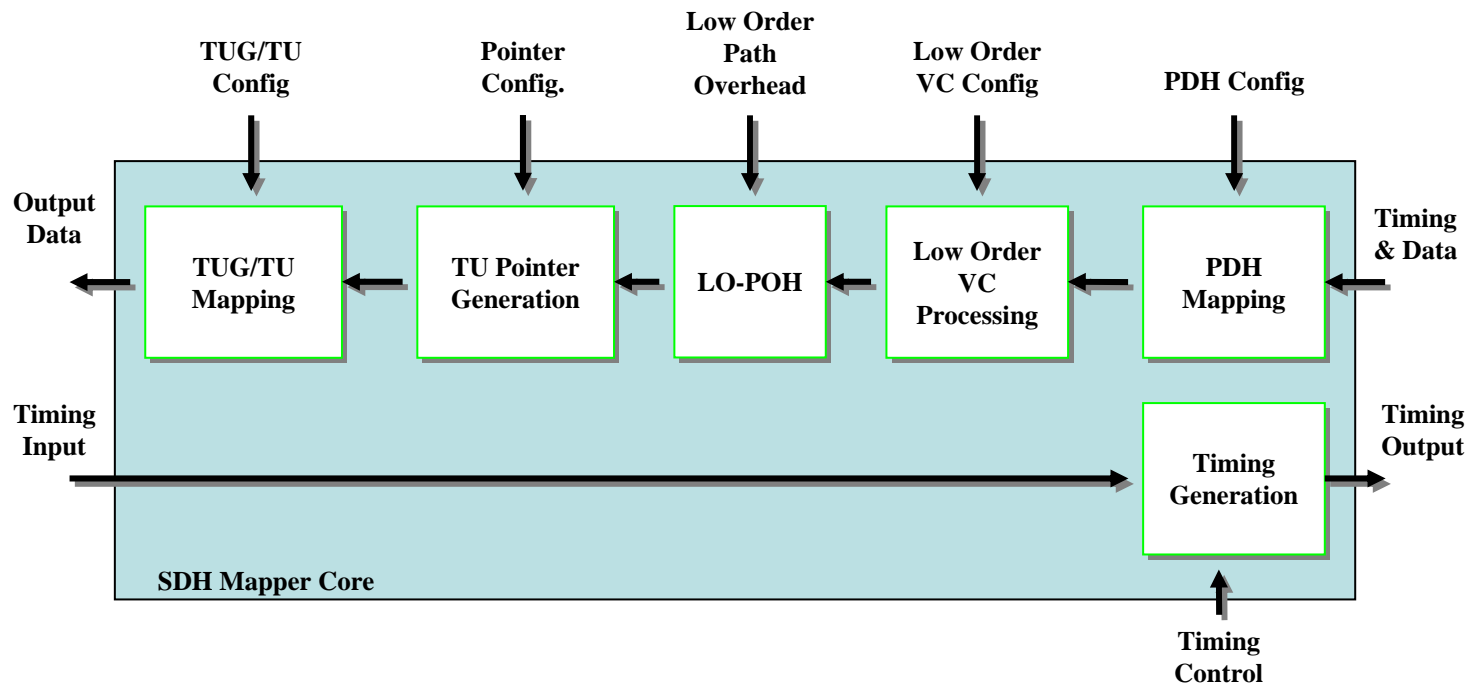


SONET/SDH Mapper STM0-4/OC1-12

- Generates up to 12 VC payloads
 - VCs can be a mix of VC3 and VC4
- Maps TUG3 into VC4 and TUG3 into VC3 or TUG3
- Maps TUs (TU11, TU12 and TU2) into TUG2
 - TU type can be dynamically configured on a per TUG2 basis
 - TU3 within TUG3 is also supported, as is VC11 over TU12
- Generates all TU pointers
 - Including the TU3 pointer for TU3 over TUG3
- Inserts all Lower-Order Path Overhead
- Calculates BIP-2 (B3 in the case of TU3 over TUG3)
- Maps PDH signals into VC and TU payloads
 - All mappings for TU11, TU12, TU2, VC3 and VC4 are supported
 - Mapping type may be dynamically configured on a per-TU/VC basis
- Accepts a multi-channel input of up to 336 TU payloads (TU11 over STM4)
- Plugs directly into SDH Framer core for a complete SDH solution
 - Also into PDH Framer cores (E1/T1 and E3/T3)



SONET/SDH Mapper STM0-4/OC1-12



Resource Utilisation (Altera)

Function	LEs	M4k	M512	Function	LEs	M4k	M512
STM-4 Deframer	1220	7	1	STM-4 Demapper	1960	10	11
STM-4 Framer	1040	7	2	STM-4 Mapper	1830	8	12

Note: Resource Utilisation figures may be improved for reduced functionality

Function	Device	LEs	M4k	M512	% used	Speed
STM-4/TU-11/12 TX & RX	EP1S25F672C7	6050	32	26	24%	90+ MHz
STM-4/TU-11/12 RX Only	EP1S10F484C7	3180	17	12	30%	90+ MHz



Resource Utilisation (Xilinx)

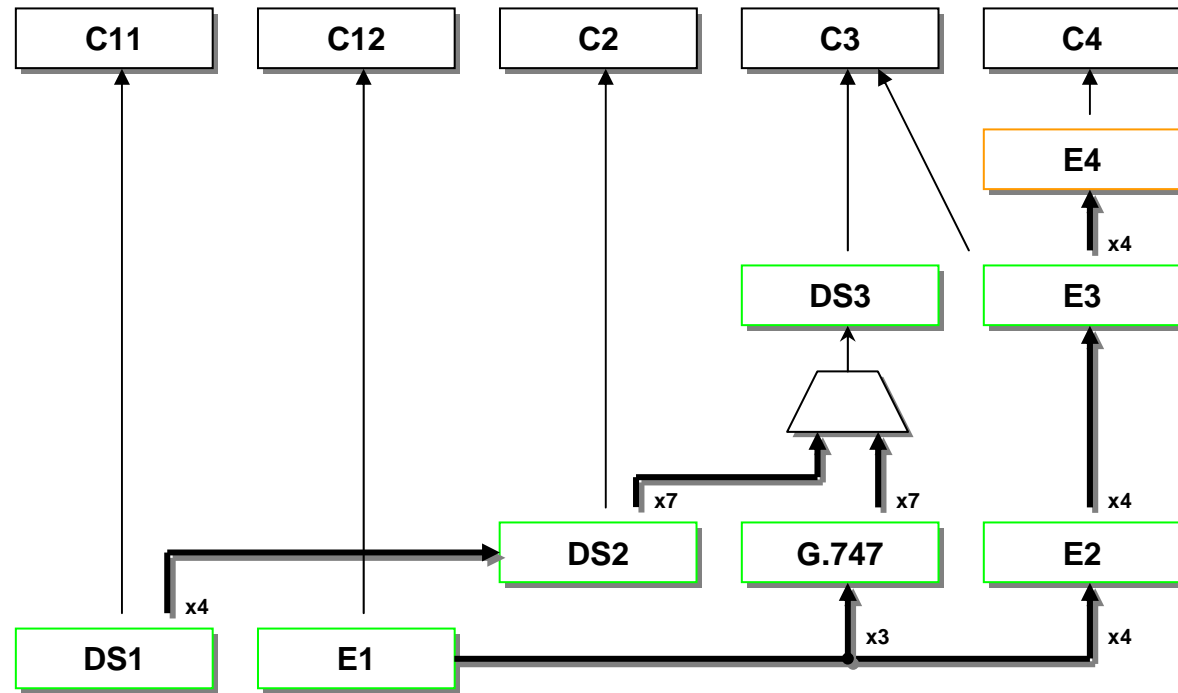
Function	Slices	BRAMs	Function	Slices	BRAMs
STM-4 Deframer	750	0	STM-4 Demapper	680	6
STM-4 Framer	500	0	STM-4 Mapper	800	5

Note: Resource Utilisation figures may be improved for reduced functionality

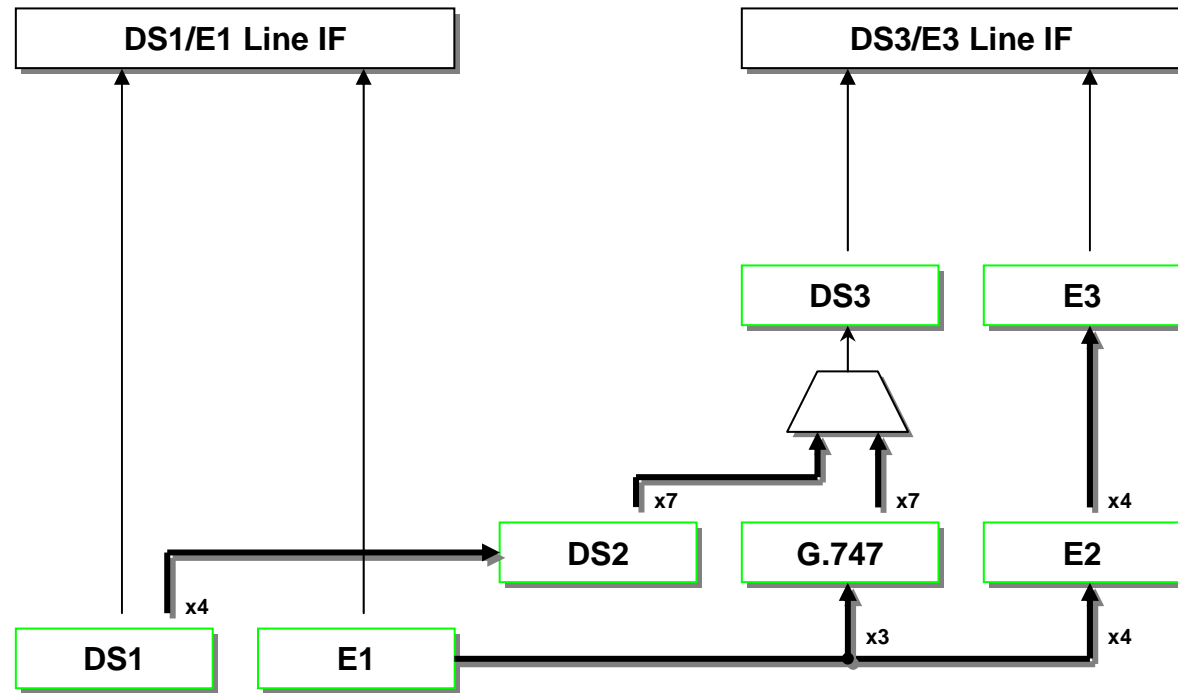
Function	Device	Slices	BRAMs	% used	Speed
STM-4/TU-11/12 TX & RX	XC2V2000FG676-4	2730	11	26%	90+ MHz
STM-4/TU-11/12 RX Only	XC2V1000FG456-4	1430	6	28%	90+ MHz



PDH Mapping IP

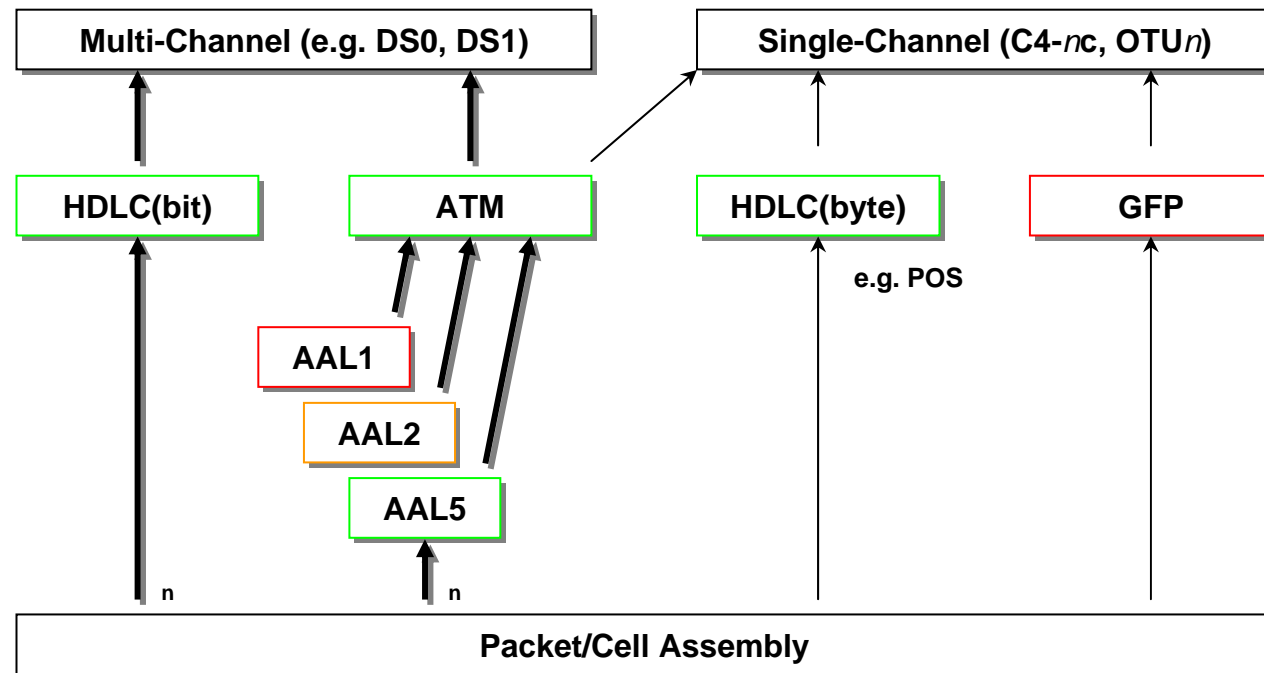


PDH Direct IP



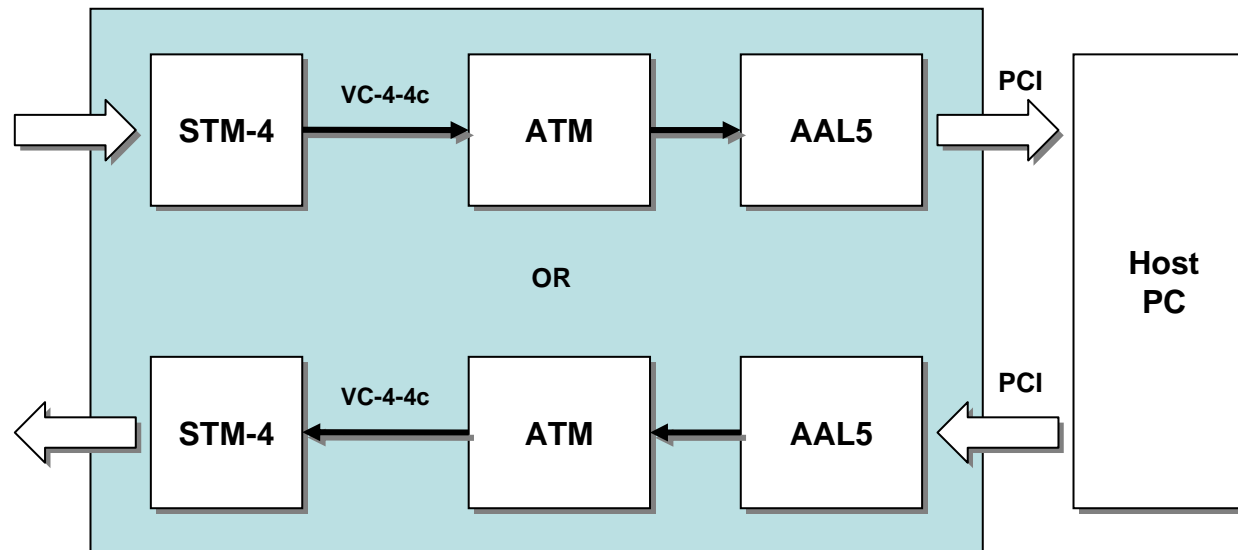
Packet/Cell IP

- Mature
- Beta
- Development



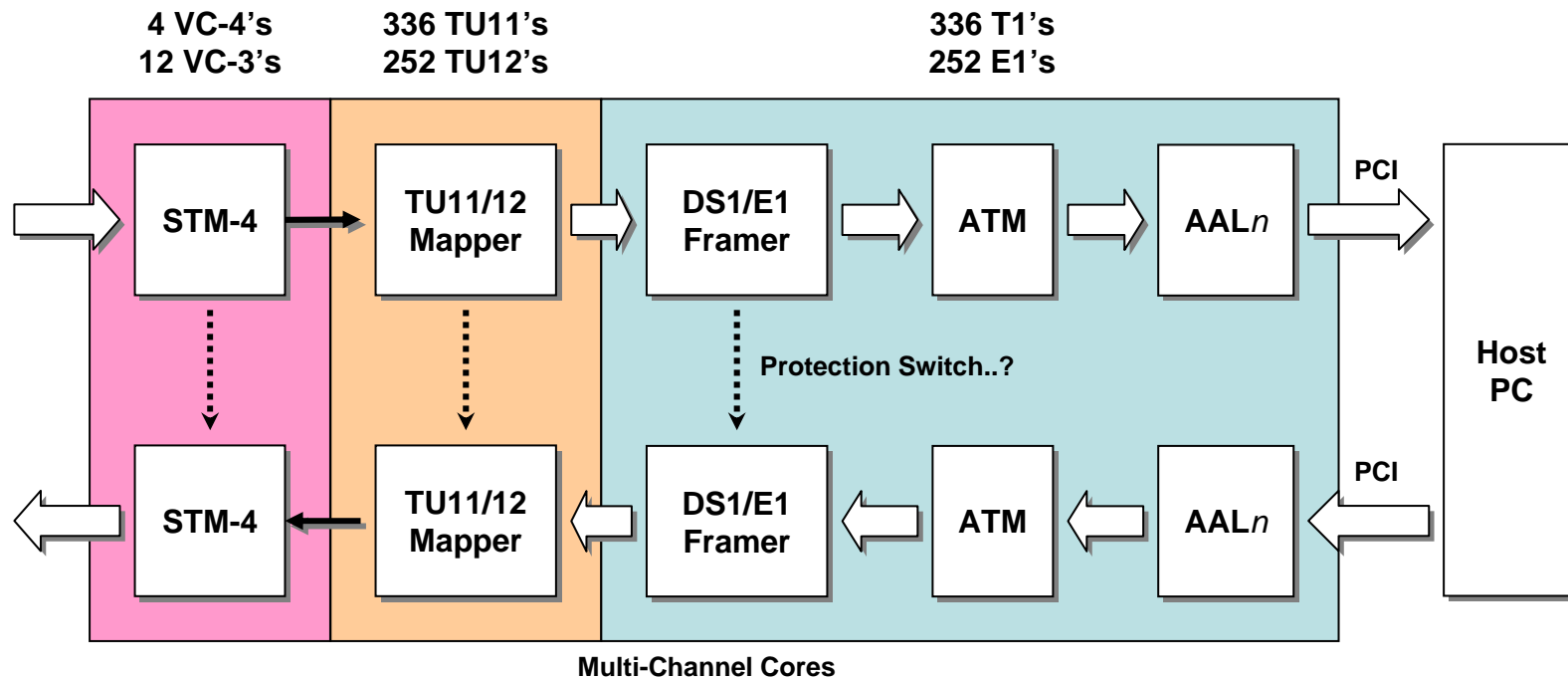
Typical Applications

- Simple ATM Packet Capture and/or ATM Traffic Generation...



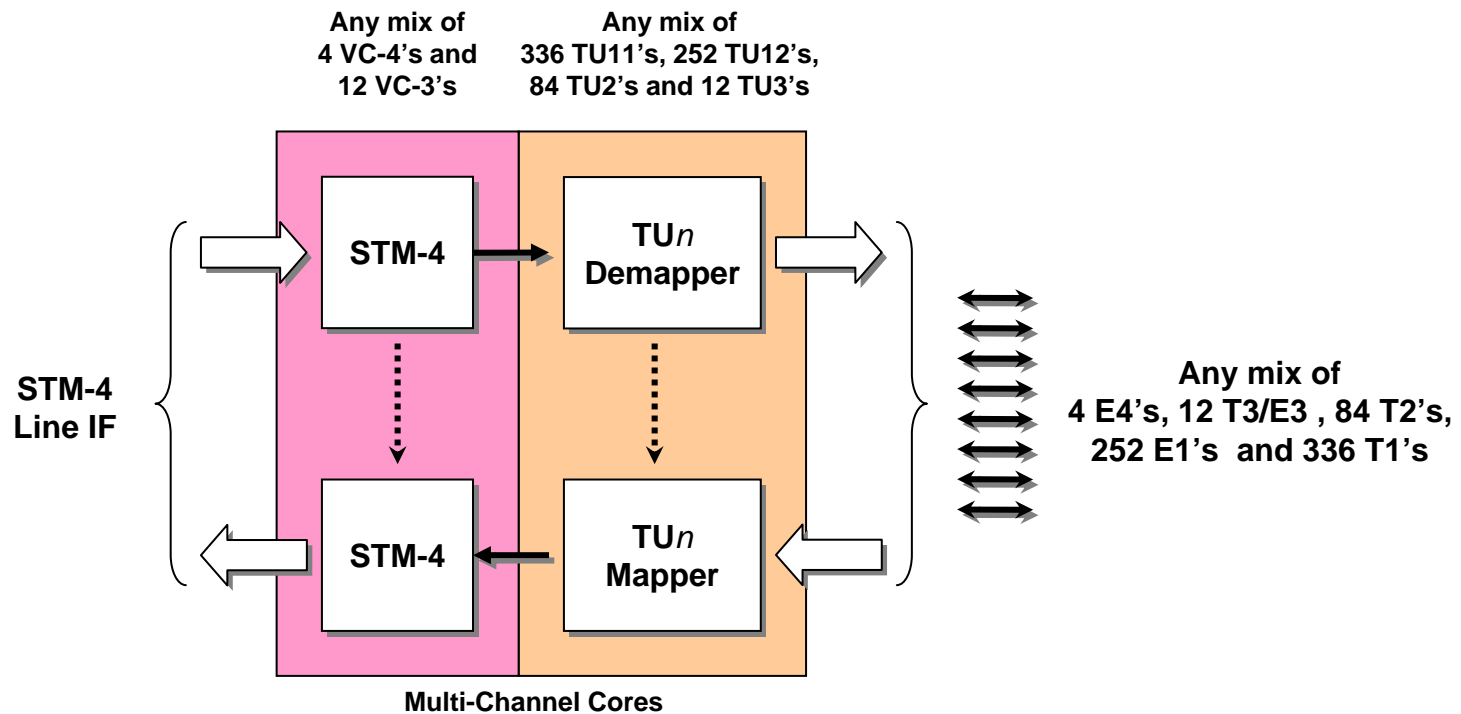
Typical Applications

- Complex 'Multi-Channel' Packet Capture and/or Generation...



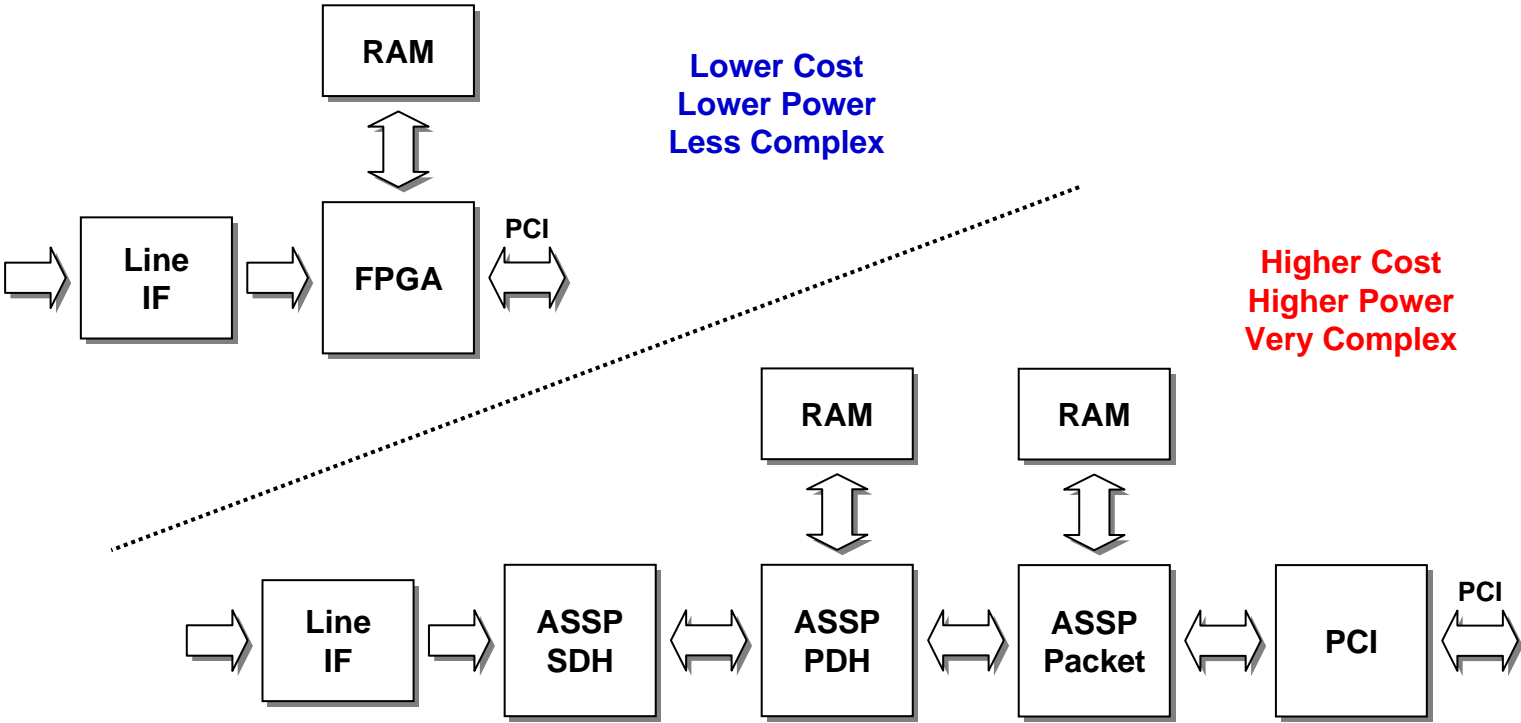
Typical Applications

- Complex Multi-Channel Mux-Demux...



Aliathon IP vs. ASSP

- Save space, cost and power while maintaining easy upgrade path...



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