High Speed - Low Latency
OTU-1 RS Encoder Core

Revision History

Version	Date	Details
Version 0.1	12.08.03	First Draft
Version 0.2	15.11.04	Updated resource utilisation
Version 0.3	17.11.04	Added Virtex4 info

Contents

1 Features

The Aliathon OTU-1 RS Encoder Core provides a very flexible, resource efficient FPGA based Core for G.709 Forward Error Correction (FEC) applications. The core:

- Is fully compatible with other supporting Aliathon Cores.
- Implements G.709 RS (255,239) OTU-1 Reed Solomon Encoding.
- Is fully synchronous and runs at very high clock speeds.
- Is available for Altera and Xilinx FPGAs.

2 Functional Description

Figure 1 illustrates the major functional blocks within the Encoder Core.

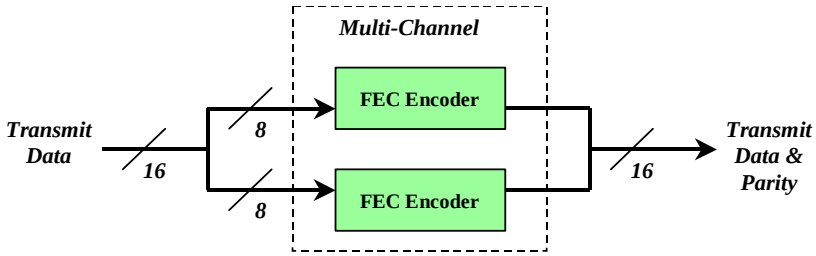

Figure 1

The Row is processed 16-bits wide and so we need 2 FEC Encoders, each handling 8 Codewords

2.1 FEC Encoder

Figure 2 illustrates the major functional blocks within the FEC Encoder.

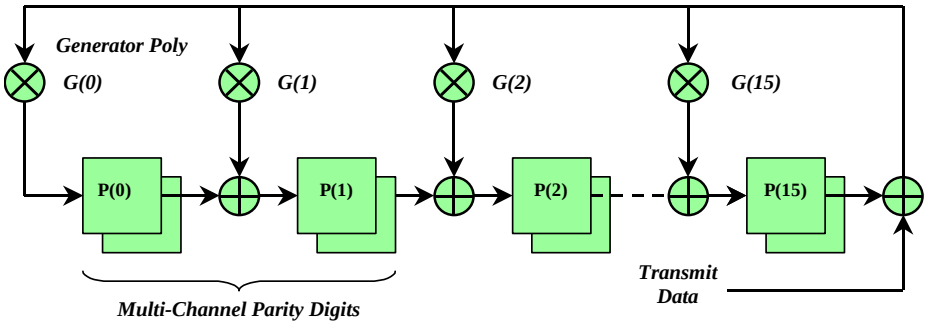

Figure 2

2.1.1 Parity

The FEC Encoder Calculates the Parity Digits for each of the 8 Interleaved Codewords. These Parity Digits are then appended to the end of the OTU-1 Row.

2.2 Performance

Since the Parity Digits are calculated as the Transmit Data is being generated, and the Digits are appended to the end of the Row, the latency of the Encoder is very low. In fact, the latency is simply the pipeline delay thru the core, which is 2 clock cycles at the Data rate.

3 Signal Description

The input and output signals are grouped by function into the following interfaces. Note that the <***ufi_data***> and <***dfo_data***> signals are 2 symbols (16-bits) wide…

3.1 Transmit Data Input Interface

This interface provides the input clock and data to the OTU-1 Encoder core.

Name	Type	Description
rst	**I**	Asynchronous reset input.
clk	**I**	**clk** is typically supplied by the external LIU. All inputs and outputs from the core are synchronous to this clock unless otherwise noted.
ufi_vld	**I**	When asserted this indicates that there is valid data on **ufi_data**. This input is useful for driving the core with data from another clock domain, via an asynchronous FIFO, for example.
ufi_data	**I**	**ufi_data** is the raw transmit data input. When **ufi_vld** is asserted it must carry valid data. Note that MSB is the first transmitted. Note that the Encoder will ignore any data in the Parity Digit positions, but still expects <**ufi_vld**> signals for those digits.
ufi_sof	**I**	When asserted this indicates that the data on **ufi_data** is the start of the transmitted OTU-1 Frame. This input is only read when **ufi_vld** asserted.

3.2 Transmit Data & Parity Output Interface

This interface provides the Output data and appended Parity from the OTU-1 Encoder.

Name	Type	Description
dfo_vld	**O**	When asserted this indicates that the following outputs are valid.
dfo_data	**O**	**dfo_data** is the transmit data with parity output. When **dfo_vld** is asserted it contains valid data. Note that MSB is the first transmitted.
dfo_sof	**O**	When asserted this indicates that the data on **dfo_data** is the start of the transmitted OTU-1 Frame. This input is only read when **dfo_vld** asserted.

3.3 Config Interface

Name	Type	Description
fec_off	**I**	When asserted the core does not insert FEC calculations.

4 Implementation Details

4.1 Resource Utilisation

The following figures are calculated assuming that all core IOs are routed off-chip. This results in a worst-case resource utilisation figure, and for any given application the resource utilisation is likely to be lower. The example parts are the mid-speed-grade, and the core exceeds performance requirements (170MHz for OTN) in these devices.

The core can be targeted for devices from other families and manufactures. Contact Aliathon for further details.

4.1.1 Altera

	Stratix Family E.g.: EP1S10F484C6			Stratix Family E.g.: EP1SGX10CF672C6		
	Used by Core	In example Part	% Utilised	Used by Core	In example Part	% Utilised
Logic Elements (LEs)	875	10570	9%	875	10570	6%
M512 RAM Blocks	16	94	18%	16	94	18%
M4k RAM Blocks	0	60	0%	0	60	0%
M-RAM Blocks	0	1	0%	0	1	0%
Fmax	>170MHz			>170MHz		

	Stratix2 Family E.g.: EP2S15F484C5		
	Used by Core	In example Part	% Utilised
ALMs	506	6240	9%
M512 RAM Blocks	16	104	16%
M4k RAM Blocks	0	78	0%
M-RAM Blocks	0	1	0%
Fmax	>170MHz		

4.1.2 Xilinx

	Virtex-II Family E.g.: XC2V1000-5FG456			Virtex-II Pro Family E.g.: XC2VP7-5FG456		
	Used by Core	In example Part	% Utilised	Used by Core	In example Part	% Utilised
Slices	846	5120	17%	846	4928	18%
BlockRAMs	0	40	0%	0	44	0%
Fmax	>170MHz			>170MHz		

	Virtex-IV Family E.g.: XC4VLX15FF668-10		
	Used by Core	In example Part	% Utilised
Slices	860	6140	15%
BlockRAMs	0	40	0%
Fmax	>170MHz		

5 Ordering Information

For technical enquiries and ordering please contact Aliathon Ltd at:

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