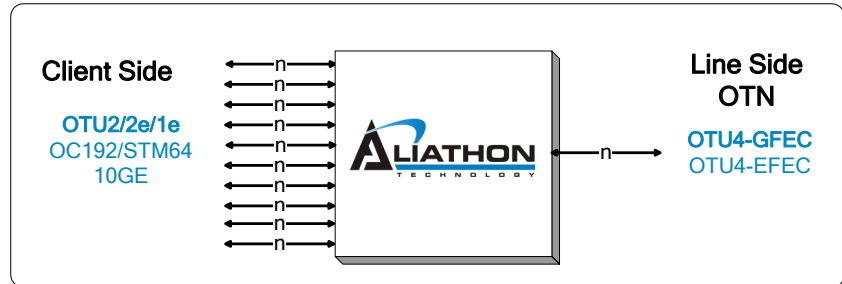


Overview

Aliathon's 10 x 10G muxponder is targeted towards the long haul OTN transport of 10G clients.

Applications include the high density aggregation of 10G clients over new DWDM links and enabling virtual data centers in the storage market.

The solution is fully ITU G.709 compliant and resides in a single FPGA.



Headline Features

- 200MHz+ push button core performance.
- All products designed from ground up to allow future datapath & channel scaling.
 - Built on technology developed at 10G & 40G rates.
 - Enabling migration path to 400G solutions in the future.
- Direct access to core registers for rapid software development.
- Errors, defects and stats provided for all client signals & OTU/ODU/OPU layers.
- Multiple 10G client interfaces with an OTL4.4 line interface.
- 10G clients mapped in to ODU2 then muxed in to ODU4 payload via the GMP.
 - Ethernet stats supported via integrated MAC & PCS layers.
- OTU4 framing and section/path overhead processing.
- Support for both standard and enhanced FEC;
 - 10G client side: G.709 GFEC & G.975.1 EFEC.
 - 100G line side: 7db NECG @ 6.7% OH G.709 GFEC.
 - 100G line side: 9.35db NECG @ 7% OH Enhanced FEC (CI-BCH-3™).

Figure 1 Overview

The client side is represented by 10 x 10G client connections. Each connection has an optional independent reference clock input (supplied by an external VCXO), enabling independent, externally controlled TX frequencies. Alternatively an FPGA based solution can be implemented. The client signals are processed by Aliathon's 10G to ODU2 mapping core, which provides support for 10G Ethernet, STM64/OC192, OTU2/2e/1e.

The 10 ODU2s from the client mapping cores connect to Aliathon's ODU2 to ODU4 mapping core, which forms a single ODU4 from the client ODU2s and passes this to the OTU4 Framing core.

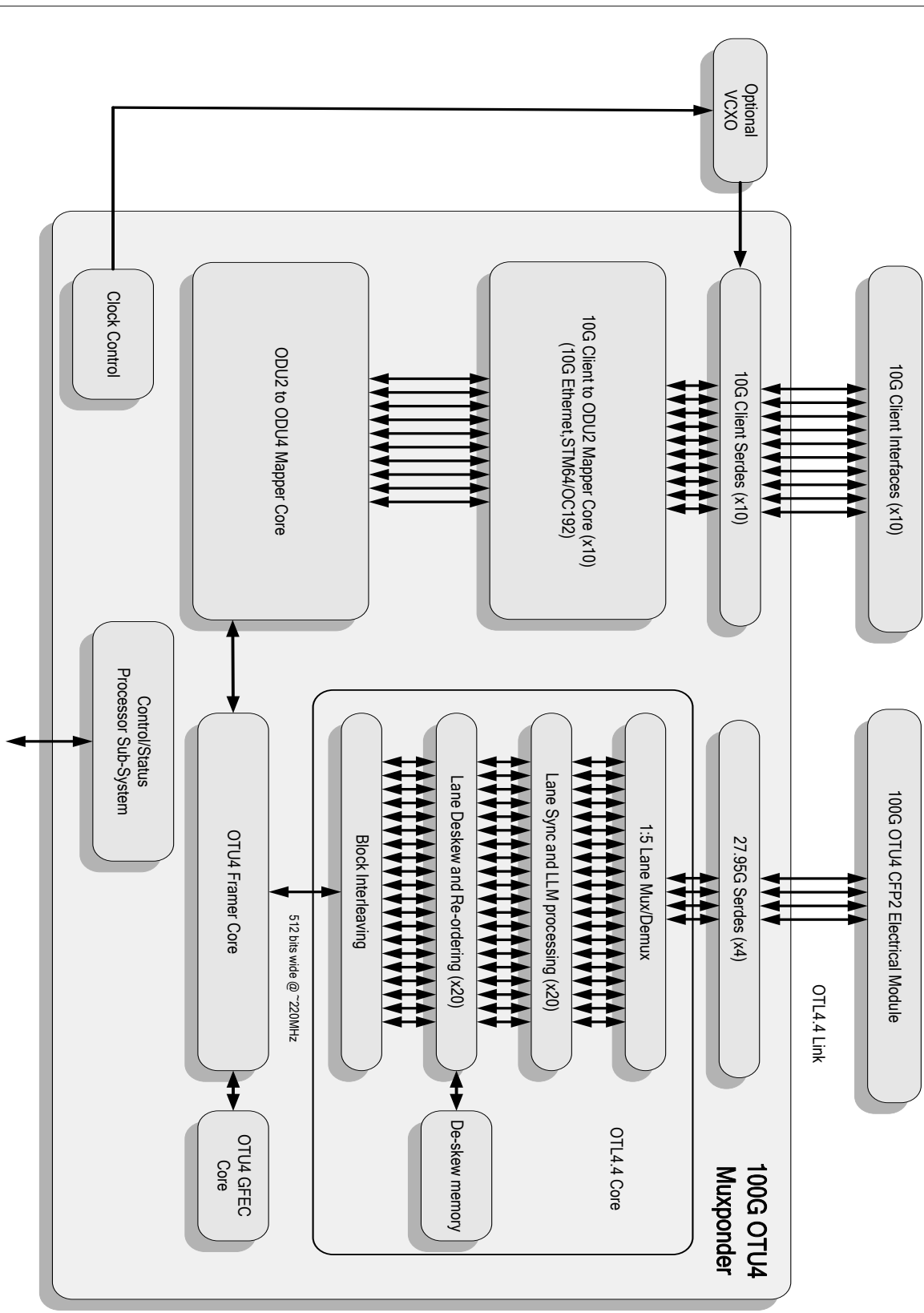
The OTU4 core provides standard G.709 OTN framing, scrambling, detection of parity errors and adds/drops the overhead.

FEC Options are;

- G.709 Standard Compliant FEC: 6.7% OH, delivering 7db of Net Electrical Coding Gain (NECG). Stats provided are corrected/uncorrected bits, blocks and codes
- Continuously Interleaved, 3-error correcting BCH (CI-BCH-3™) eFEC - 7% OH, delivering 9.35db of Net Electrical Coding Gain (NECG). Stats provided are corrected/uncorrected bits, blocks and codes

On the OTU4 side the design implements an OTL4.4 interface (up to 1024bits of skew matching the IEEE MLD Requirement). This incorporates 4 x 27.95G SERDES with individual lane framing (based on the OTU4 FAS pattern and the inserted LLM bytes), skew adjustment and reordering.

Figure 1: Architectural Block Diagram



OTN Overhead Alarms Supported / Processed

Frame

- OOF: Out of Frame (FAS error).
- LOF: Loss of Frame (OOF persistence).
- OOM: Out of Multiframe (MFAS error).
- LOM: Loss of Multiframe (OOM persistence).

OTU Section Monitoring

- SM-BIP-8: SM Bit Interleaved Parity.
- SM-BEI: SM Backward Error Indication.
- OTU-AIS: OTU Alarm Indicator Signal.
- SM-BDI: SM Backward Defect Indicator.
- SM-IAE: SM Incoming Alignment Error.
- SM-BIAE: SM Backward Incoming Alignment Error

ODU Path Monitoring & TCM

- PM-BIP-8: PM BIP Error
- PM-BEI: PM Backward error Indication.
- ODU-AIS: ODU Alarm Indicator Signal.
- ODU-OCI: ODU Open Connection Indication.
- ODU-LCK: ODU Lock Defect.
- PM-BDI: PM Backward Defect Indication.
- PM-TIM: Trace Identified Mismatch.
- TCMi-BIP-8, TCMi-BEI, TCM-BDI, TCM-BIAE, TCM-AIS, TCM-OCI, TCM-LCK, TCM-LTC, TCM-IAE, TCM-TIM.

OPU

- PTM: Payload Type Mismatch
- CSF: Client Signal Fail.

Target Families & Deliverables

Altera

- Stratix

Xilinx

- Virtex

IP

- EDIF/BIT/SOF/QSF/UCF. Encrypted ModelSim & Back annotated VHDL

Documentation

- Datasheet, Verification Results, User Guide.

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