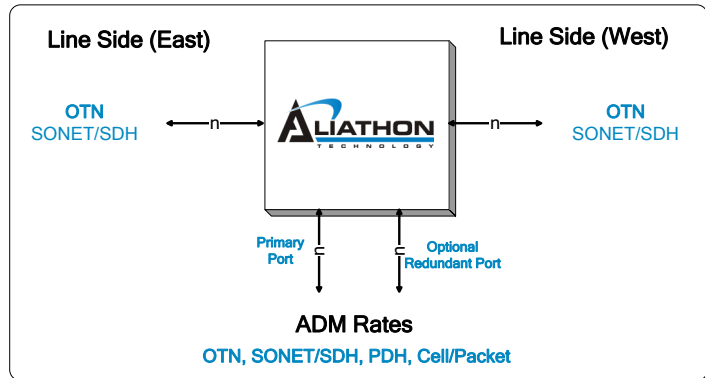


Overview

Aliathon's 100G add/drop multiplexor is targeted towards the next generation metro ring topologies for OTN.

Applications include the high density multiplexing of 10G clients into and out of 100G transport pipes in the emerging coherent detection, metro market.

The solution is fully ITU G.709 compliant and resides in a single FPGA.



Headline Features

- 200MHz+ push button core performance.
- All products designed from ground up to allow future datapath & channel scaling.
 - Built on technology developed at 10G & 40G rates, enabling a migration path to 400G solutions in the future.
- Direct access to core registers for rapid software development.
- Errors, defects and stats supported for all client signals.
- OTU4 framing and section/path overhead processing.
- Multiple 10G client interfaces with an OTL4.10 east / west interface. 10G clients mapped in to ODU2 then muxed in to ODU4 payload via the GMP.
- ODU2 client signals (real & redundant) switched via Aliathon's high speed 400G cross-connect.
- Support for both standard and enhanced FEC;
 - 10G client side: G.709 GFEC & G.975.1 EFEC.
 - 100G line side: 7db NECG @ 6.7% OH G.709 GFEC or 9.35db NECG @ 7% OH Enhanced FEC (CI-BCH-3™).

Figure 1 Overview

The client sides (primary & optional redundant) are represented by 10 x 10G client connections. Each connection has an optional independent reference clock input (supplied by an external VCXO), enabling independent, externally controlled TX frequencies. Alternatively an FPGA based solution can be implemented. Client add/drop is supported via this flexible clocking architecture.

The client signals are processed by Aliathon's 10G to ODU2 mapping core, which provides support for 10G Ethernet, STM64/OC192, OTU2/2e/1e/2f/1f.

All ODU's from the client mapping cores connect to Aliathon's 400G capacity ODU cross-connect which routes these signals to either the East or West line side interface. The switch is intelligently configured to compensate for network failures in traditional ring topologies.

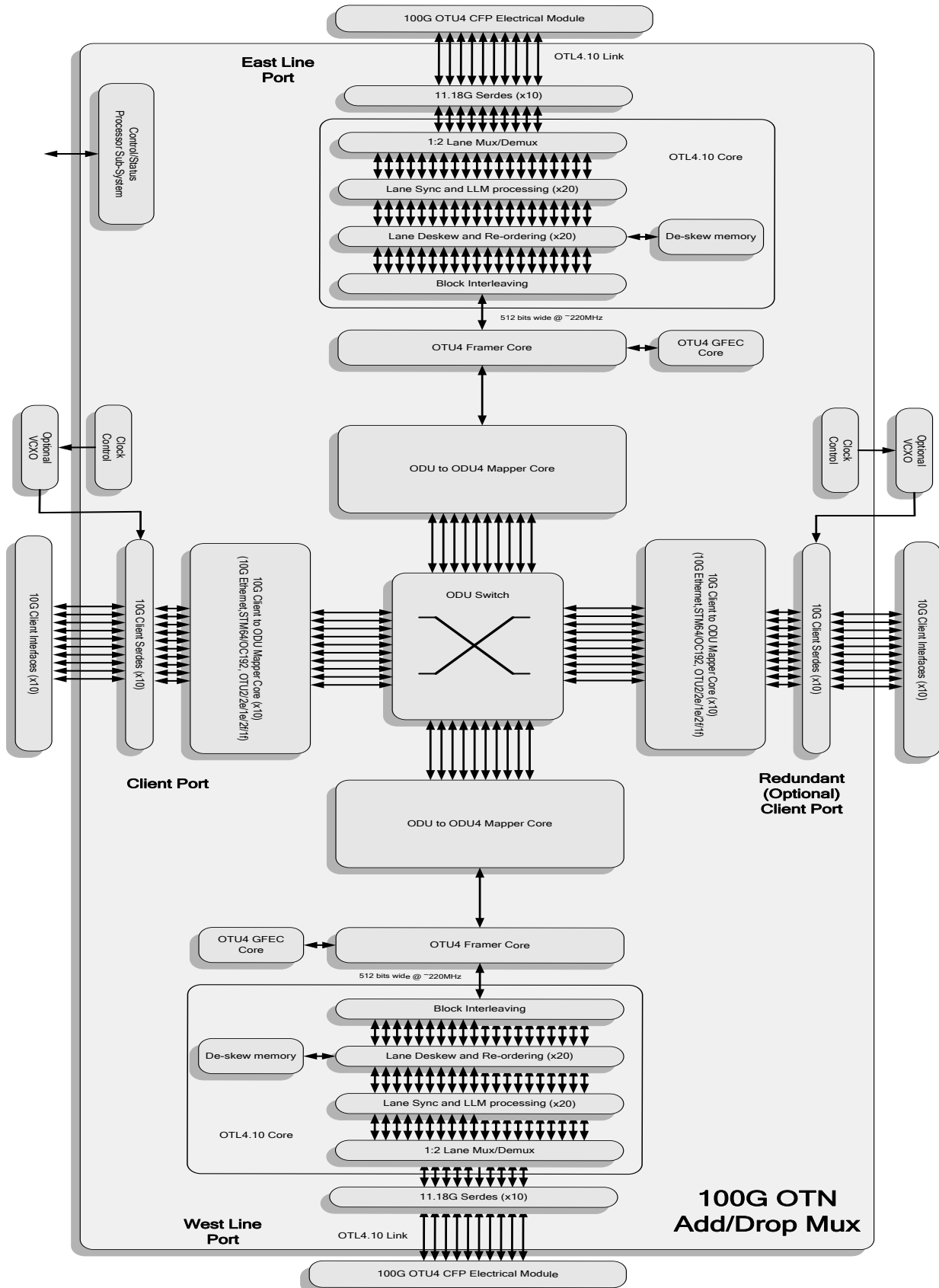
On the East & West line sides the design implements an OTL4.10 interface (up to 1024-bits of skew matching the IEEE MLD Requirement). This incorporates 10 x 11.18G SERDES with individual lane framing (based on the OTU4 FAS pattern and the inserted LLM bytes), skew adjustment and reordering. This core interfaces directly to Aliathon's OTU4 Framer/FEC blocks.

The OTU4 core provides standard G.709 OTN framing, scrambling, detection of parity errors and adds/drops the overhead.

FEC Options are;

- G.709 Standard FEC: 6.7% OH, 7db NECG. Stats provided are corrected/uncorrected bits, blocks & codes.
- Continuously Interleaved, 3-error correcting BCH (CI-BCH-3™) eFEC - 7% OH, 9.35db NECG. Stats provided are corrected/uncorrected bits, blocks & codes.

Figure 1: Architectural Block Diagram



100G OTN
Add/Drop Mux

OTN Overhead Alarms Supported / Processed

Frame

- OOF: Out of Frame (FAS error).
- LOF: Loss of Frame (OOF persistence).
- OOM: Out of Multiframe (MFAS error).
- LOM: Loss of Multiframe (OOM persistence).

OTU Section Monitoring

- SM-BIP-8: SM Bit Interleaved Parity.
- SM-BEI: SM Backward Error Indication.
- OTU-AIS: OTU Alarm Indicator Signal.
- SM-BDI: SM Backward Defect Indicator.
- SM-IAE: SM Incoming Alignment Error.
- SM-BIAE: SM Backward Incoming Alignment Error

ODU Path Monitoring & TCM

- PM-BIP-8: PM BIP Error
- PM-BEI: PM Backward error Indication.
- ODU-AIS: ODU Alarm Indicator Signal.
- ODU-OCI: ODU Open Connection Indication.
- ODU-LCK: ODU Lock Defect.
- PM-BDI: PM Backward Defect Indication.
- PM-TIM: Trace Identified Mismatch.
- TCMi-BIP-8, TCMi-BEI, TCM-BDI, TCM-BIAE, TCM-AIS, TCM-OCI, TCM-LCK, TCM-LTC, TCM-IAE, TCM-TIM.

OPU

- PTM: Payload Type Mismatch
- CSF: Client Signal Fail.

Target Families & Deliverables

Altera

- Stratix

Xilinx

- Virtex

IP

- EDIF/BIT/SOF/QSF/UCF. Encrypted ModelSim & Back annotated VHDL

Documentation

- Datasheet, Verification Results, User Guide.

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