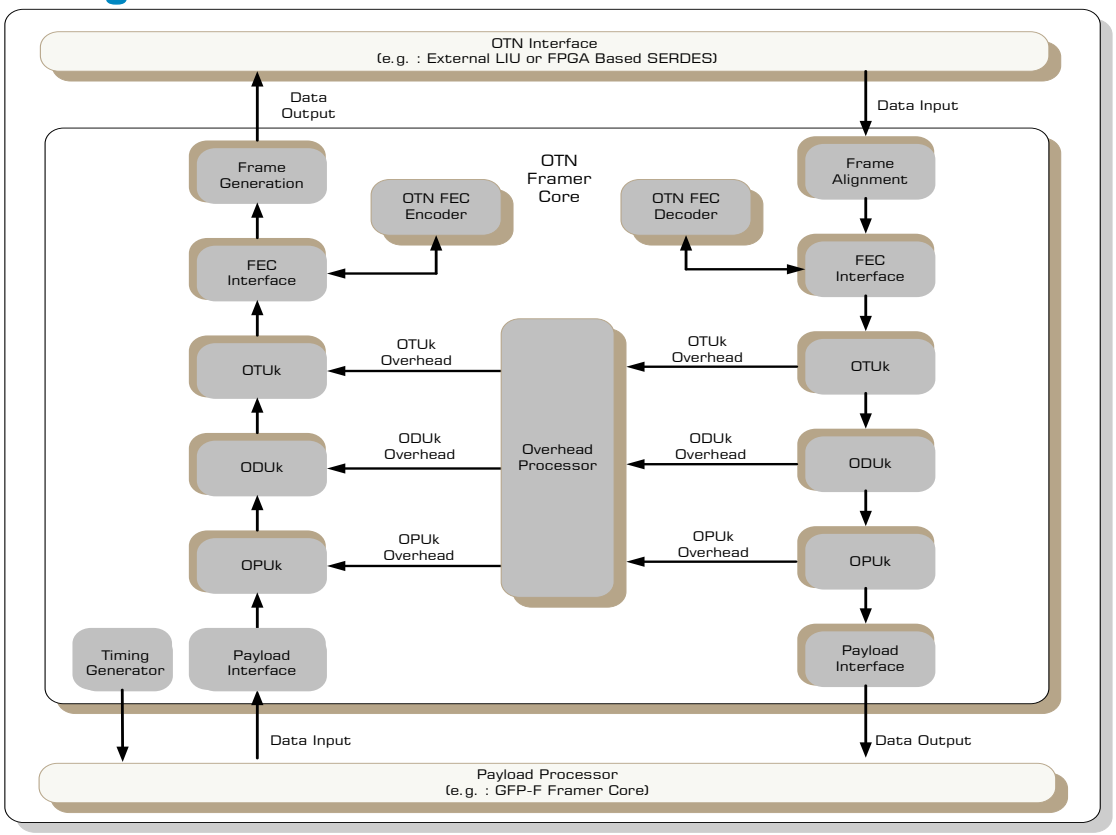
OTN Framer
Product Brief

Overview

Aliathon's OTN Framer Core implements OTU, ODU and OPU layer functions and provides an integrated Reed-Solomon FEC codec in a flexible, resource-efficient FPGA based solution. Running at 166.62MHz or above, it is available for OTU1, OTU2 and OTU3 rates. OTU4 is under development.

Block Diagram



Resources

- Conforms to G.709.
- Generates the OTN frame structure and inserts framing overhead; detects and aligns to the OTN framing pattern.
- Processes the OTN frame, OTUk Overhead, and Section Monitoring BIP. Processes ODUk Overhead, calculates and detects Path Monitoring BIP.
- Supports synchronous payload mappings (eg: ATM, GFP), and asynchronous SONET/SDH mappings (accommodating positive/negative stuffing).
- Detects LOS, LOF, MF-LOF, OTU AIS and ODU AIS, OCI and LCK defects.
- Supports a contiguous payload interface: 16 bits wide for OTU1, 64 bits wide for OTU2, 256 bits wide for OTU3
- Implements G.709 (255,239) OTN Reed Solomon encoding and low latency (27µs) decoding. Flags all corrected bits, symbols and indicates uncorrectable codewords.
- Full Overhead and Defect processing including:
  - LOS, LOF, MF-LOF.
  - **OTUk Section Monitoring** with TTI, BIP-8, BDI, BEI/BIAE. **ODUk Path Monitoring** with TTI, BIP-8, BDI, BEI, STAT (LCK, OCI, AIS). **ODUk Tandem Connection Monitoring** (TCM1-6) with TTI, BIP-8, BDI, BEI/BIAE, STAT(LCK,OCI,AIS). **OPUk** PSI and PT.
  - Performance Monitoring counters (OTUk-BIP, ODUk-PM-BIP, ODUk-TCM-BIPs, BEI, corrected symbols, uncorrectable words).

OTN Framer
Product Brief

Resources

Rate	OTU1	OTU2	OTU3
Framer (Tx)			
FFs	1255	contact	contact
LUTs (4-Input)	830	contact	contact
Memory (kbit)	2.1	contact	contact
Deframer (Rx)			
FFs	2085	contact	contact
LUTs (4-Input)	3795	contact	contact
Memory (kbit)	213.6	contact	contact
OH Processor			
FFs	1300	contact	contact
LUTs (4-Input)	1100	contact	contact
Memory (kbit)	40	contact	contact
Total			
FFs	4640	contact	contact
LUTs (4-Input)	5725	contact	contact
Memory (kbit)	255.7	contact	contact
Fmax (2)			
> 170 MHz			

Deliverables	
IP	EDIF/BIT/SOF file
Simulation	Encrypted Modelsim Back-annotated VHDL
Constraints	QSF or UCF
Documentation	Datasheet

Target families
Altera – Stratix, Arria and Cyclone
Xilinx – Virtex, Kintex, Artix and Spartan
Lattice – ECP2/M and ECP3

1 - Guideline Utilization figures are based on an average sample of the supported architectures and may increase.
Memory implementation is device dependent and figures may increase on less memory efficient architectures.
Memory figures may be reduced at the expense of logic on some architectures.
2 - Guideline Performance figures are based on the slowest Speed Grade of the high performance devices and may be less for slower, lower cost, devices.

Contact Us

info@aliathon.com

+44 (0)1383 737 736

www.aliathon.com

Aliathon Ltd

Evans Business Center

Pitreavie Court

Dunfermline, Fife, KY11 8UU

Scotland, UK

Alliances

ALTERA AMPP SM
ALTERA MEGAFUNCTION PARTNERS PROGRAM

XILINX
ALLIANCE PROGRAM

Mentor Graphics