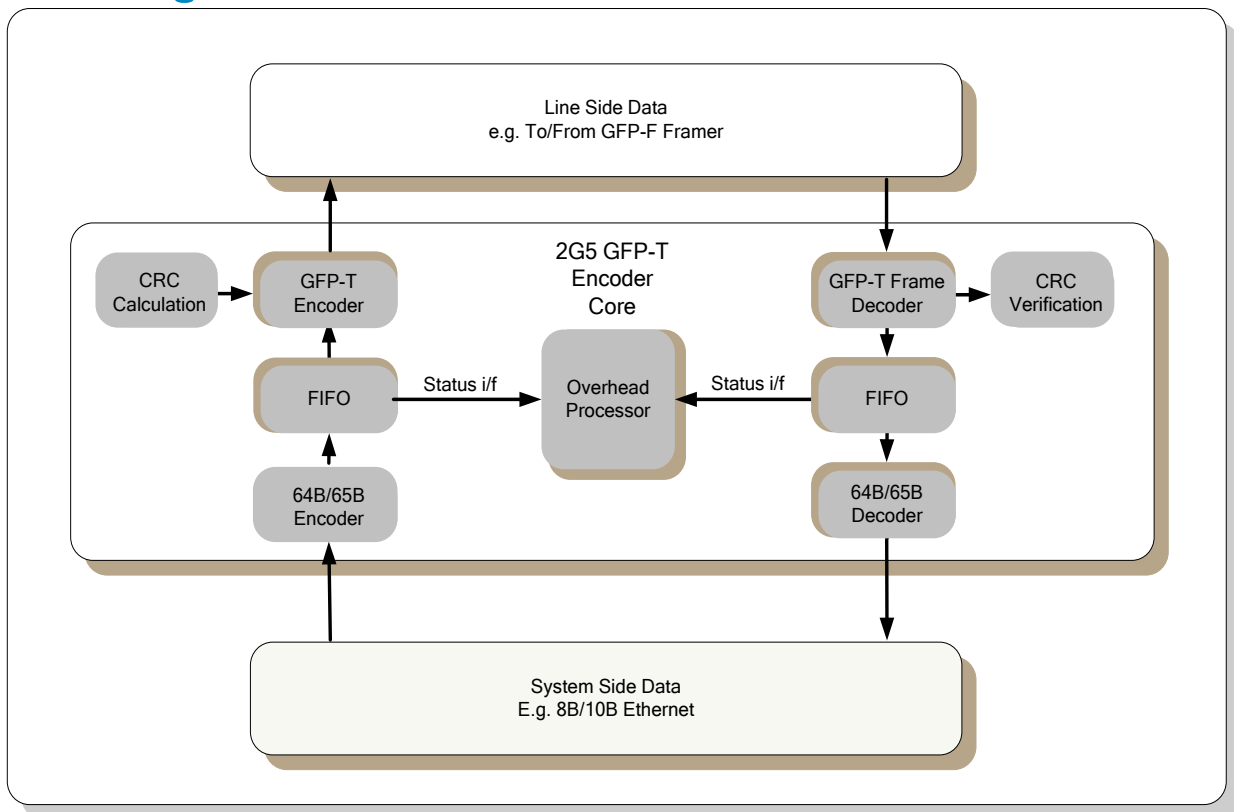


Overview

Aliathon's 2.5Gbps GFP-T Encoder Core provides a flexible, resource-efficient, high-density programmable logic based solution for GFP interfacing.

The core encodes 8B/10B signals and maps them into fixed length transparent GFP blocks. The Core also simultaneously extracts the 8B/10B signals from received GFP-T blocks.

Block Diagram



Key Features

- Compliant with ITU-T G.7041 specification.
- Best-in-Class size and performance. Multiple FPGA vendor support.
- Accepts 64 byte blocks of data from an 8B/10B data source.
- Encodes input blocks into 67 byte GFP-T blocks as per G.7041.
- Calculates block CRC-16 and verifies block CRC-16.
- Extracts 64 byte 8B/10B blocks of data from GFP-T frames.
- Supports multiple blocks per GFP frame.
- Supports multiple channels using GFP Extension Header channel ID.
- Inserts/detects 10B_ERR code for unrecognised K characters. Inserts/detects 65B_PAD code for rate adaptation.
- Interfaces to Aliathon's GFP Framer core for GFP transmission.
- Overhead and Defect processing including:
 - CRC error.
 - Performance Monitoring Counter (CRC).

Resources

Framer (Tx)	
FFs	530
LUTs (4-Input)	820
Memory (kbit)	2.2
Deframer (Rx)	
FFs	1610
LUTs (4-Input)	1650
Memory (kbit)	1.2
OH Processor	
FFs	100
LUTs (4-Input)	100
Memory (kbit)	1
Total (1)	
FFs	2240
LUTs (4-Input)	2570
Memory (kbit)	4.4
Fmax (2)	
> 170 MHz	

Deliverables	
IP	EDIF/BIT/SOF file
Simulation	Encrypted Modelsim Back-annotated VHDL
Constraints	QSF or UCF
Documentation	Datasheet

Target families	
Altera – Stratix, Arria and Cyclone	
Lattice – ECP2/M and ECP3	
Xilinx – Virtex, Kintex, Artix and Spartan	

1 - Guideline Utilization figures are based on an average sample of the supported architectures and may increase.


Memory implementation is device dependent and figures may increase on less memory efficient architectures.

Memory figures may be reduced at the expense of logic on some architectures.

2 - Guideline Performance figures are based on the slowest Speed Grade of the high performance devices and may be less for slower, lower cost, devices.

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