SONET/SDH Framer
Product Brief

Overview

Aliathon's SONET/SDH Framer Core implements Transport Overhead framing functions for SONET/SDH links, including frame generation and delineation, protection switching, concatenated and channelized Higher Order Path termination and defect/overhead processing.

It provides a flexible, resource-efficient, FPGA based solution for interfacing to one or more SONET/SDH links, such as

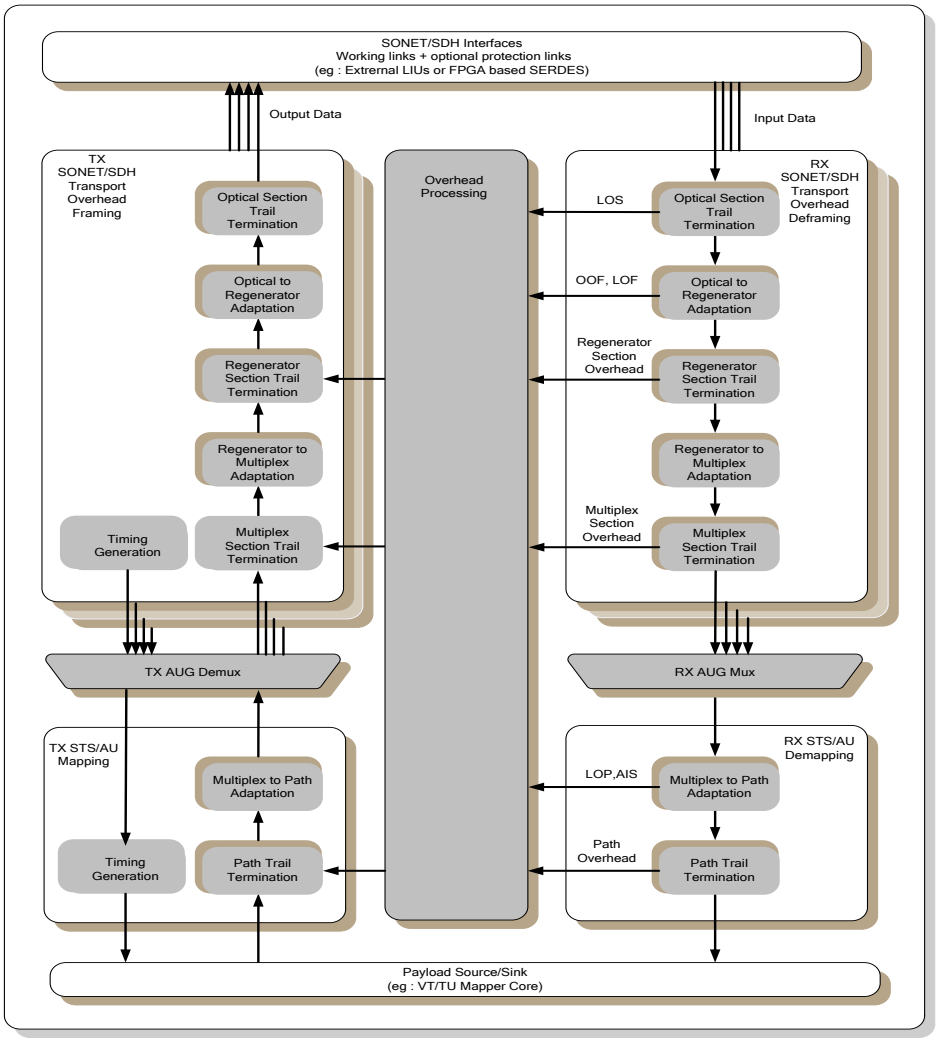
1 x OC3/STM1,

8 x OC3/STM1 and

2 x OC12/STM4,

or 1 x OC192/STM16.

Block Diagram



Key Features

- Conforms to G.707, G.806, G.783 and T1.105
- Interfaces to the following SONET/SDH links:
  - OC1/STM0, OC3/STM1, OC12/STM4, OC48/STM16, OC192/STM64
- Performs frame generation, delineation and scrambling for one or multiple links.
- Detects Loss of Signal (LOS), Out of Frame (OOF) and Loss of Frame (LOF) defects.
- Extracts Regenerator/Multiplex Overhead and detects B1 and B2 errors.
- Implements MS protection switching. Processes all STS/AU pointers and Higher Order paths.
- Detects AIS and LOP defects, and B3 BIP errors.
- All legal configurations of STS/VC sizes are supported, and may be changed dynamically.
- Full Overhead and Defect processing for all TOH and STS/VC, including:
  - LOF, OOF, B1, B2, MS-AIS/RDI, MS-REI, AU-AIS/LOP and Path B3, REI, RDI. Trace Messages (J0, J1). Signal Degrade/Excessive Error detection (B2, B3). Path Labels (S1, C2). Performance Monitoring counters (B1, B2, MS-REI, Path B3 and REI). Upstream/Downstream Consequent Action.

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Example Applications		LUTs (4 input)	FFs	Memory (kbit)
1 x OC3/STM1	RX	1305	1175	0.75
Max. 3 STS/VC paths	TX	695	840	0.25
	Oh. Proc[2]	2817	2690	23.7
A_SDHFRM1_1	**Total (1)**	**4817**	**4705**	**24.7**
4 x OC3/STM1	RX	3470	3500	3.8
1 x OC12/STM4	TX	1890	1895	1.4
Max. 12 STS/VC paths	Oh. Proc[2]	3361	2919	58.6
A_SDHFRM4_4	**Total (1)**	**8721**	**8314**	**63.8**
8 x OC3/STM1	RX	6320	6470	6.4
2 x OC12/STM4	TX	3295	3275	1.7
Max. 24 STS/VC paths	Oh. Proc[2]	4067	3220	71
A_SDHFRM8_8	**Total (1)**	**13682**	**12965**	**79.1**
1 x OC48/STM16	RX	2415	2385	6.3
Max. 48 STS/VC paths	TX	1222	1085	3.3
	Oh. Proc[2]	2971	2716	151.6
A_SDHFRM16_1	**Total (1)**	**6686**	**6186**	**161.2**
1 x OC192/STM64	RX	4350	4010	9.5
1 x STS192c/Vc4-16c path	TX	1810	2295	6.3
	Oh. Proc[2]	2775	2682	20.8
A_SDHFRM64c_1	**Total (1)**	**8935**	**8987**	**36.6**
Fmax(3)				
> 160 MHz				

Deliverables	
IP	EDIF/BIT/SOF file
Simulation	Encrypted Modelsim Back-annotated VHDL
Constraints	QSF or UCF
Documentation	Datasheet

Target families
Altera – Stratix, Arria and Cyclone
Xilinx – Virtex, Kintex, Artix and Spartan
Lattice – ECP2/M and ECP3

1 - Guideline Utilization figures are based on an average sample of the supported architectures and may increase. Memory implementation is device dependent and figures may increase on less memory efficient architectures. Memory figures may be reduced at the expense of logic on some architectures.
2 - If Trace Message and SD/EXC processing is not required the OH Processor Memory figure reduces by 50%.
3 - Guideline Performance figures are based on the slowest Speed Grade of the high performance devices and may be less for slower, lower cost, devices.

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