Overview

Aliathon’s VT/TU Mapper performs the insertion and extraction of PDH signals into or from multiple VT/TU paths. The core handles pointer generation and signal insertion into the transmitted paths as well as the pointer alignment and signal extraction from the received paths. It also performs the lower order path overhead processing for both directions.

Running at over 160MHz, and processing hundreds of Independently configurable TX and RX VT/TU paths concurrently.

Block Diagram

Key Features

- Conforms to ITU G.707/ANSI T1.105.
- Maps/Demaps multiple Lower Order VT/TU paths:
  - VC3 - TUG2 - (TU11 / TU12 / TU2)
  - VC4 - TUG3 - TUG2 - (TU11 / TU12 / TU2)
  - VC4 - TUG3 - TU3
  - STS1 - VCG - (VT1.5 / VT2 / VT6)
- Inserts/Extracts PDH signals for VT/TU and STS/VC containers:
  - DS1 over VT1.5/TU11 or VT2/TU12
  - E1 over VT2/TU12
  - DS2 over VT6/TU2
  - DS3/E3 over STS1/VC3
  - E4 over STS3c/VC4
- Generates/Processes all VT/TU pointers. Calculates and inserts TX VT/TU BIP values. Provides a Path Overhead Insert/drop interface.
- All legal configurations of VT/TU sizes supported, and can be changed dynamically. Supports independent timing of STS/VC inputs/outputs.
- Full Overhead and Defect processing per VT/TU including:
  - LOP, AIS, BIP, eRDI-P/S/C, RFI, REI and LOMF.
  - Trace Messages (J2).
  - Signal Degrad/Excessive Error detection (BIP).
  - Path Label (V5-PL).
  - Performance Monitoring Counters (BIP, REI)
  - Upstream/Downstream Consequent Action.
1 - Guideline Utilization figures are based on an average sample of the supported architectures and may increase. Memory implementation is device dependent and figures may increase on less memory efficient architectures. Memory figures may be reduced at the expense of logic on some architectures. 

2 - If the OH Processor uses memory external to the FPGA the OH Processor Memory figure reduces by 50%

3 - If Trace Message and SD/EXC processing is not required the OH Processor Memory figure reduces by 50%

4 - Guideline Performance figures are based on the slowest Speed Grade of the high performance devices and may be less for slower, lower cost, devices.

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Mentor Graphics