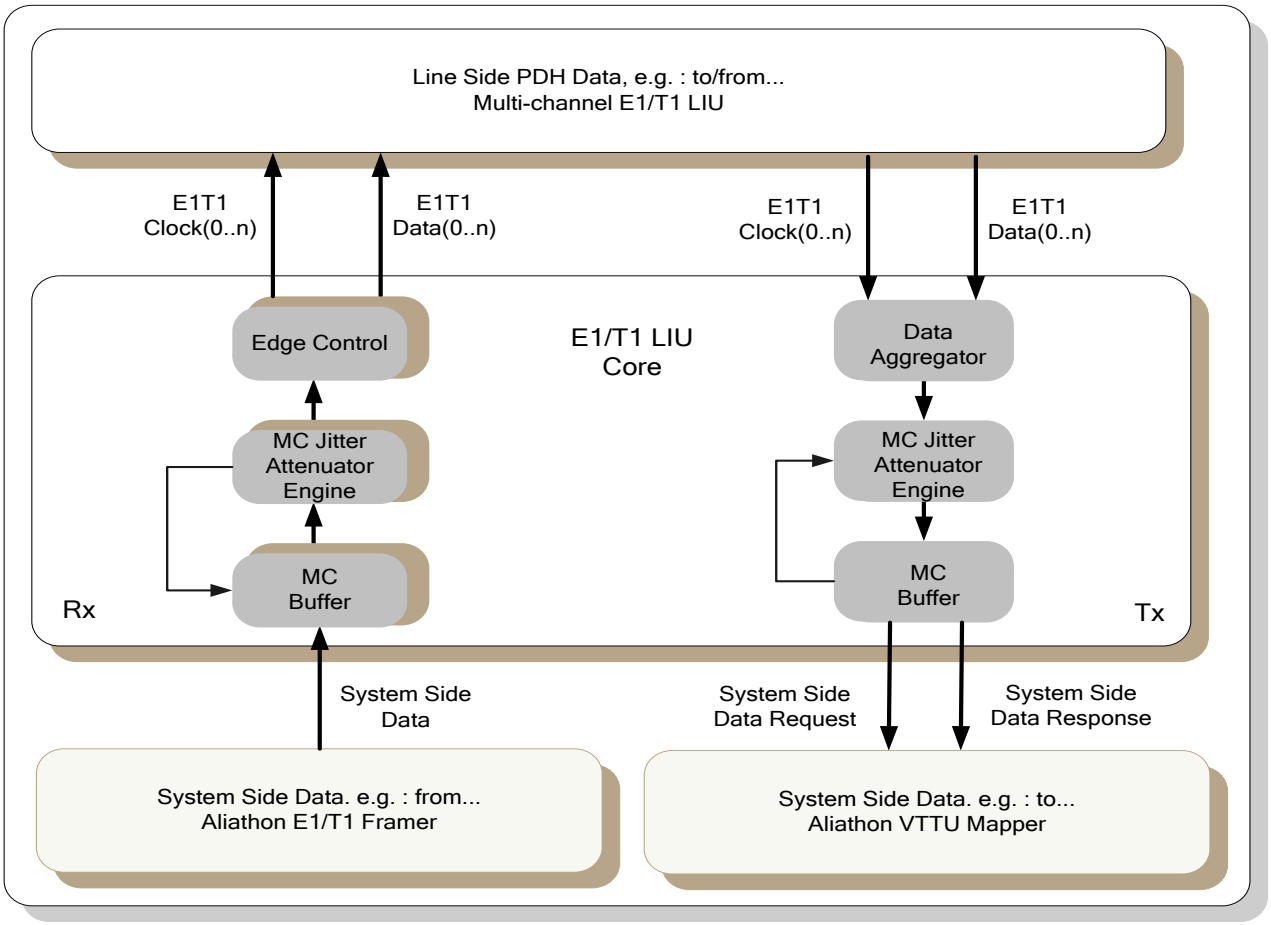
e1t1 Line Interface Unit / Framer
Product Brief

Overview

Aliathon's Multi-Channel E1/T1 Line Interface Core provides a flexible, resource-efficient, high-density programmable logic based solution for PDH Line interfacing. Running at 155MHz, it is capable of attenuating jitter for up to 504/672 E1/T1 channels (2xOC12/2xSTM4 links).

Block Diagram



Key Features

- Best-in-Class size and performance and supports many hundreds of channels.
- Provides multi-channel Jitter Attenuation in the receive and transmit paths.
- Supports E1 and T1 rates. Fully synchronous and runs at high speeds.
- Designed to provide G.832 and G.824 Output Jitter Compliance, capable of attenuating 2.048 kHz +/-50 ppm (E1), 1.544 kHz +/-32 ppm (T1)
- Accepts multiple input streams, making it ideal for interfacing to E1/T1 demappers. The input streams may dynamically range between 1 and 8 bits wide, allowing seamless interfacing to PDH mappings.
- Supports independent timing on every channel.
- In the Rx direction generates up to 504/672 independent serial/data lines for the attenuated E1/T1s.
- In the Rx direction data can be configured to change in the rising or falling edge of the clock.
- Glueless connection to Aliathon E1/T1 Framer (in the Rx direction) and Aliathon VTTU mapper (in the Tx direction).
- Fully adaptable by Aliathon to meet your requirements depending on the reference clock and the number of channels you need to attenuate.

e1t1 Line Interface Unit / Framer
Product Brief

Resources

Example Applications		LUTs (4 input)	FFs	Memory (kbit)
28xT1s 21xE1s	RX	600	550	3.8
	TX	317	339	4.8
	Total (1)	**917**	**889**	**8.6**
84xT1s 63xE1s	RX	1800	1650	11.4
	TX	631	856	19.1
	Total	**2431**	**2506**	**30.5**
168xT1s 126xE1s	RX	3000	3300	22.8
	TX	1200	1200	25
	Total	**4200**	**4500**	**47.8**
336xT1s 252xE1s	RX	4900	5500	46
	TX	2474	1819	30.5
	Total (1)	**7374**	**7319**	**76.5**
672xT1s 504xE1s	RX	contact	contact	contact
	TX	contact	contact	contact
	Total (1)	contact	contact	contact
Fmax(2)				
> 160 MHz				

Deliverables	
IP	EDIF/BIT/SOF file
Simulation	Encrypted Modelsim Back-annotated VHDL
Constraints	QSF or UCF
Documentation	Datasheet

Target families
Altera – Stratix, Arria and Cyclone
Xilinx – Virtex, Kintex, Artix and Spartan
Lattice – ECP2/M and ECP3

1 - Guideline Utilization figures are based on an average sample of the supported architectures and may increase.
Memory implementation is device dependent and figures may increase on less memory efficient architectures.
Memory figures may be reduced at the expense of logic on some architectures.

Contact Us

info@aliathon.com

+44 (0)1383 737 736

www.aliathon.com

Aliathon Ltd

Evans Business Center

Pitreavie Court

Dunfermline, Fife, KY11 8UU

Scotland, UK

Alliances

ALTERA AMPP SM
ALTERA MEGAFUNCTION PARTNERS PROGRAM

XILINX
ALLIANCE PROGRAM

Mentor Graphics