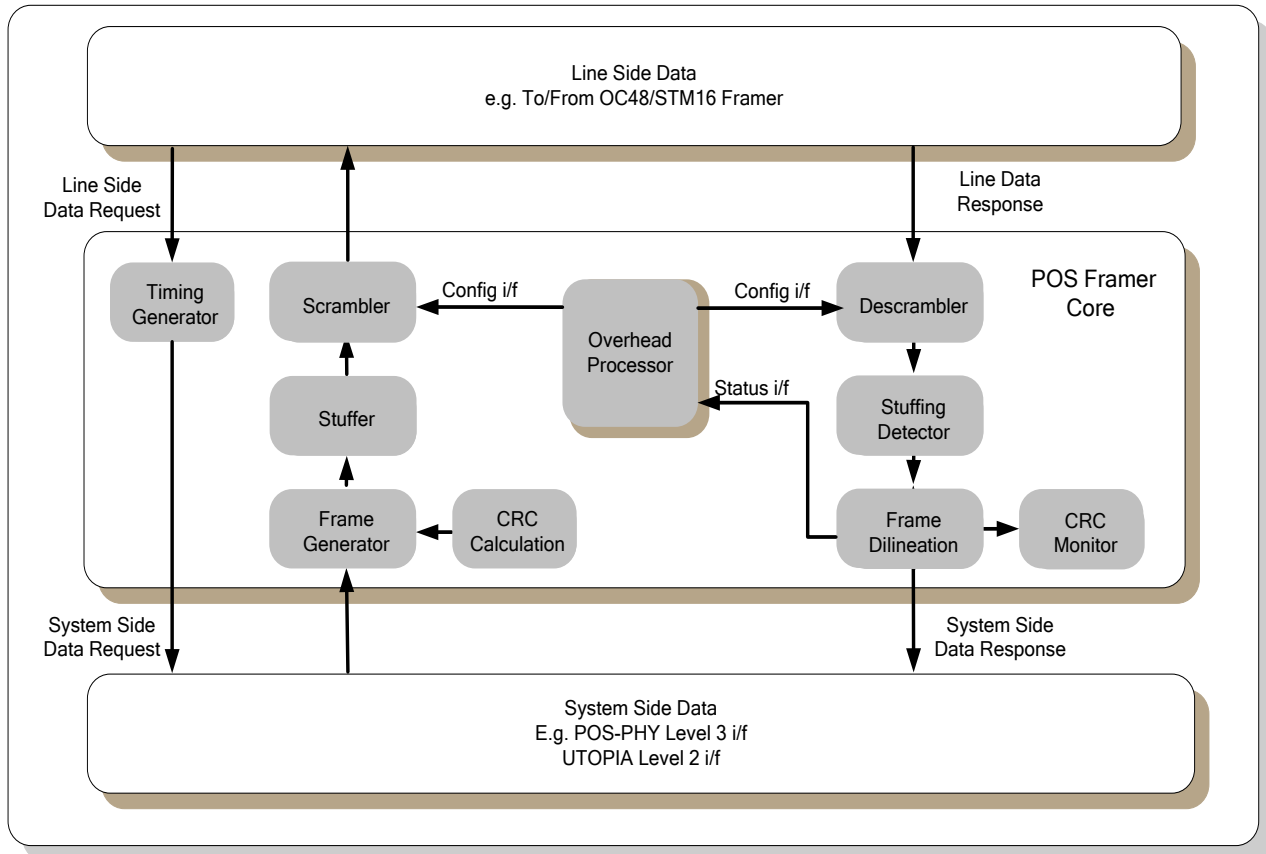


Overview

Aliathon's Packet Over SONET/SDH (PoS) Framer Core provides a flexible, resource-efficient, high-density programmable logic based solution for PoS interfacing. Running at up to 155.52MHz, it is capable of PoS frame processing for data streams up to 10Gbps.

Block Diagram



Key Features

- Best-in-Class size and performance.
- Multiple FPGA vendor support.
- Available for the following SONET/SDH rates:
 - OC1/STM0, OC3/STM1, OC12/STM4, OC48/STM16, OC192/STM64
- Processes data stream byte stuffing.
- Generates flag characters for inter-frame gaps.
- Inserts and detects CRC-16 and CRC-32.
- Scrambles and descrambles the data stream using the $X^{43} + 1$ polynomial.
- Indicates CRC, abort, alignment and frame-length errors.
- Ideal for FPGA-based systems processing PoS over concatenated SONET/SDH.
- Interfaces directly with SONET/SDH framer cores and bus interface cores (POS-PHY3).
- Overhead and Defect processing including:
 - Frame Abort, CRC, Length Error Indicators.
 - Performance Monitoring Counters (CRC, Frame Abort).

Resources

	STM4	STM16	STM64
Framer (Tx)			
FFs	160	645	1910
LUTs (4-Input)	270	870	3125
Memory (kbit)	0	27.6	104
Deframer (Rx)			
FFs	150	470	2140
LUTs (4-Input)	315	615	3200
Memory (kbit)	0	0	69.3
OH Processor			
FFs		100	
LUTs (4-Input)		150	
Memory (kbit)		1	
Total (1)			
FFs	410	1215	4150
LUTs (4-Input)	735	1635	6475
Memory (kbit)	1	28.6	174.3
Fmax (2)			
> 160 MHz			

Deliverables	
IP	EDIF/BIT/SOF file
Simulation	Encrypted Modelsim Back-annotated VHDL
Constraints	QSF or UCF
Documentation	Datasheet

Target families
Altera – Stratix, Arria and Cyclone
Lattice – ECP2/M and ECP3
Xilinx – Virtex, Kintex, Artix and Spartan

1 - Guideline Utilization figures are based on an average sample of the supported architectures and may increase.

Memory implementation is device dependent and figures may increase on less memory efficient architectures.

Memory figures may be reduced at the expense of logic on some architectures.

2 - Guideline Performance figures are based on the slowest Speed Grade of the high performance devices and may be less for slower, lower cost, devices.

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