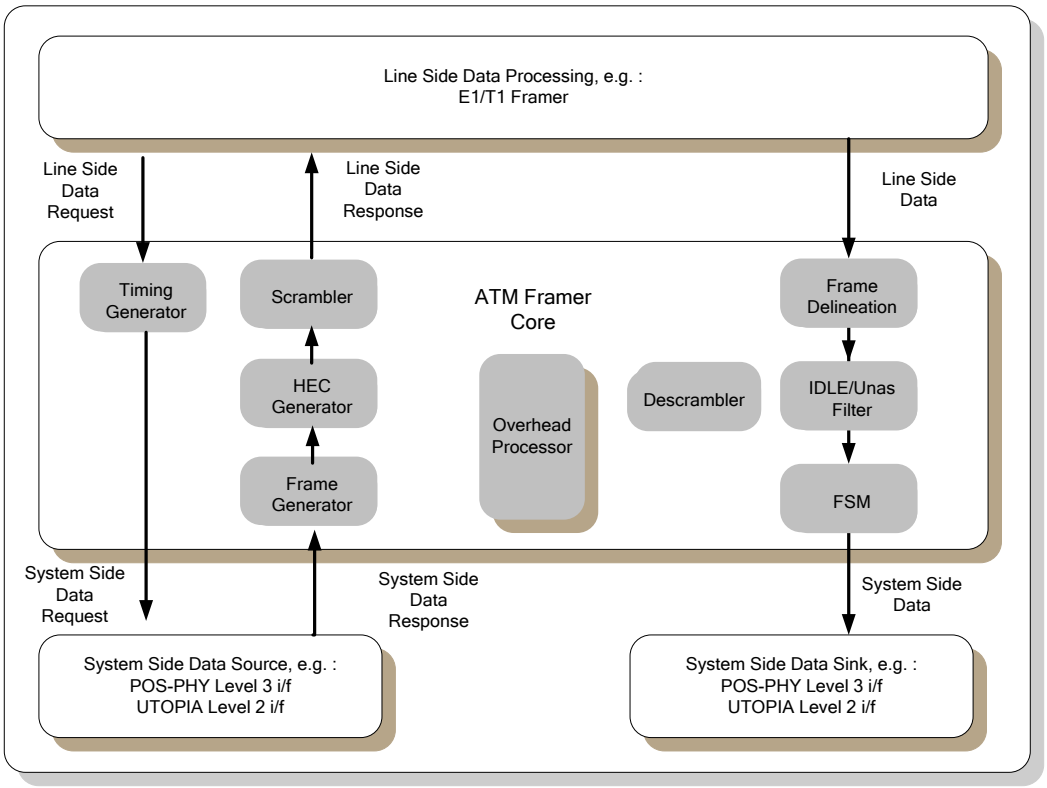
ATM Framer
Product Brief

Overview

Aliathon's ATM Framer Core provides a flexible, resource-efficient, high-density programmable logic based solution for ATM interfacing. Running at 155MHz, it is capable of processing thousands of ATM channels.

Block Diagram



Resources

- Conforms to ITU I.432.1.
- Best-in-Class size and performance. Supports many thousands of channels.
- Multiple FPGA vendor support.
- Processes data for multiple independent TDM ATM streams.
- Configurable IDLE and Unassigned Cell insertion, detection and deletion.
- Optional HEC insertion; HEC error detection and correction.
- Supports multiple stream processing for glueless interfacing in multi-channel PDH systems.
- Supports dynamically ranged streams between 1 and 8 bits wide.
- Byte wide interface allows easy interface to Aliathon's OC3/STM1, OC12/STM4 and 2xOC12/STM4 channelized systems.
- Configuration may be applied to each stream independently, and changed dynamically.
- Full Overhead and Defect processing per channel including:
  - LCD, Uncorrectable HEC, Correctable HEC, Good HEC, IDLE detected.
  - Performance Monitoring counters (Uncorrectable HEC, Correctable HEC, Good HEC).

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Channels (c)	512	1024	4096
Framer (Tx)			
FFs	420		
LUTs(4-Input)	325		
Memory (kbit)	39.5	78.9	315
Deframer (Rx)			
FFs	240		
LUTs (4-Input)	650		
Memory (kbit)	55.3	110.6	443
OH Processor			
FFs	400		
LUTs(4-Input)	300		
Memory (kbit) (2)	76	147	580
Total			
FFs	1060		
LUTs (4-Input)	1275		
Memory (kbit) (2)	170.8	336.5	1338
Fmax (3)			
> 160 MHz			

Deliverables	
IP	EDIF/BIT/SOF file
Simulation	Encrypted Modelsim Back-annotated VHDL
Constraints	QSF or UCF
Documentation	Datasheet

Target families
Altera – Stratix, Arria and Cyclone
Xilinx – Virtex, Kintex, Artix and Spartan
Lattice – ECP2/M and ECP3

1 - Guideline Utilization figures are based on an average sample of the supported architectures and may increase.
Memory implementation is device dependent and figures may increase on less memory efficient architectures.
Memory figures may be reduced at the expense of logic on some architectures.
2 - If the OH Processor uses external memory to the FPGA the OH Processor Memory figure reduces by 70%.

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