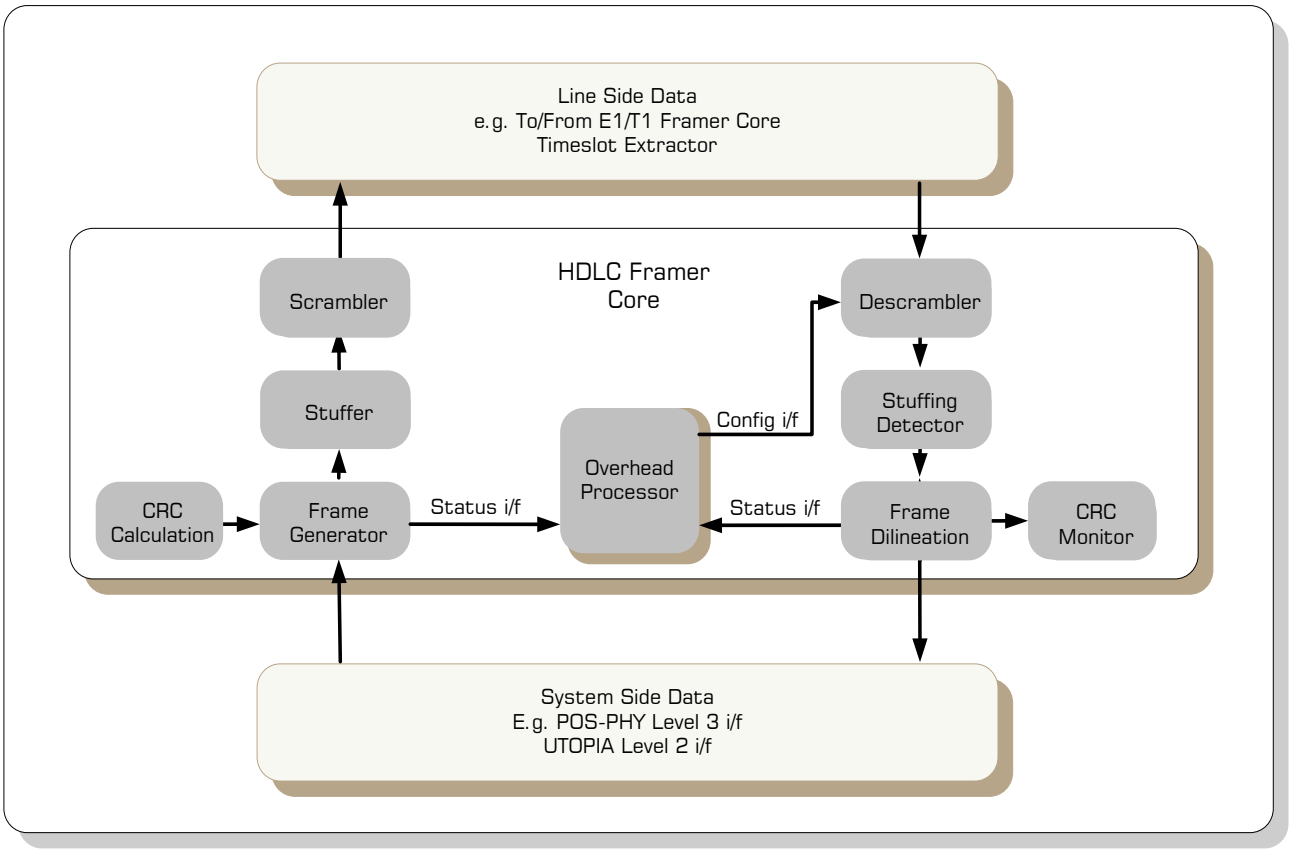
HDLC Framer
Product Brief

Overview

Aliathon's HDLC Framer Core provides a flexible, resource-efficient, high-density programmable logic based solution for HDLC interfacing. Running at over 155MHz, it is capable of generating and deframing thousands of HDLC channels.

Block Diagram



Key Features

- Best-in-Class size and performance, supports many thousands of channels.
- Supports bit-synchronous and byte-synchronous HDLC.
- Generates/Accepts data for multiple independent TDM HDLC streams. Generates/Removes flag characters to delineate HDLC frames.
- Inserts/Removes HDLC bit or byte stuffing. Provides variable width data output.
- Calculates/Verifies and inserts CRC-16 and CRC-32.
- Scrambles/Descrambles the data stream using the $X^{43}+1$ polynomial.
- Indicates CRC, abort, alignment and frame-length errors.
- Outputs/Accepts frame-aligned payload bytes.
- The line-side input/output data may dynamically range between 1 and 8 bits wide, allowing seamless interfacing to synchronous and asynchronous PDH framers.
- Configuration may be applied to each stream independently, and changed dynamically.
- Full Overhead and Defect processing per channel including:
    - Frame Abort, CRC, Non Byte-Aligned, Length Error Indicators. Performance Monitoring Counters (CRC, Frame Abort).

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Channels (c)	512	1024	4096
Framer (Tx)			
FFs	410		
LUTs (4-Input)	520		
Memory (kbit)	23	46	184
Deframer (Rx)			
FFs	710		
LUTs (4-Input)	635		
Memory (kbit)	37.9	75.8	303.1
OH Processor			
FFs	400		
LUTs (4-Input)	300		
Memory (kbit) **(2)**	58	116	466
Total (1)			
FFs	1520		
LUTs (4-Input)	1455		
Memory (kbit) **(2)**	118.9	237.8	953.1
Fmax (3)			
> 160 MHz			

Deliverables	
IP	EDIF/BIT/SOF file
Simulation	Encrypted Modelsim Back-annotated VHDL
Constraints	QSF or UCF
Documentation	Datasheet

Target families
Altera – Stratix, Arria and Cyclone
Xilinx – Virtex, Kintex, Artix and Spartan
Lattice – ECP2/M and ECP3

1 - Guideline Utilization figures are based on an average sample of the supported architectures and may increase.
Memory implementation is device dependent and figures may increase on less memory efficient architectures.
Memory figures may be reduced at the expense of logic on some architectures.
2 - If the OH Processor uses external memory to the FPGA the OH Processor Memory figure reduces by 65%.

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XILINX
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Mentor Graphics