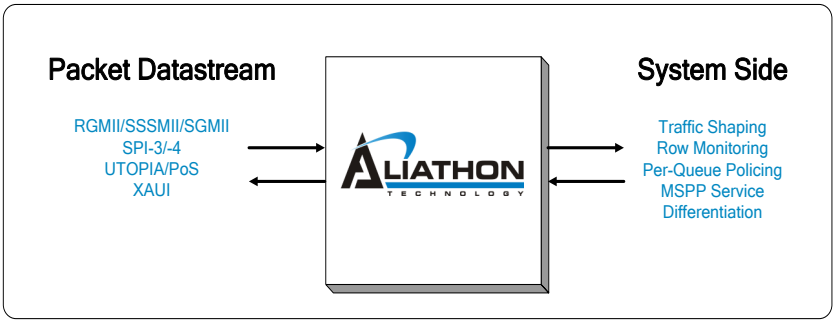
Packet Classifier

Product Brief

Overview

Aliathon's Packet Classification core is targeted at replacing expensive & power hungry Network Processors (NPUs) and Content Addressable Memory (CAM) for high speed, exact match look-up in the optical network packet domain.

The solution is highly scalable to fit applications from 155M - 100G and resides in a single FPGA.



Headline Features

- 200MHz+ push button core performance.
- Designed from the ground up to allow future protocol and channel/key scaling.
- Fully compliant with Aliathon's existing solutions;
  - 155M, 622M, 2.5G and 10G SONET/SDH (inc. PDH) solutions.
  - 2.5G, 10G, 100G OTN solutions.
- Input key support from 256K to 1M.
- Fully deterministic lookup table performance up to 80Gbps.
- Fast in-band system update for dynamic rule-set support.
- Complete multi-protocol packet classification and stream ID assignment based on configurable input keys including;
  - IPv4/IPv6 addresses.
  - MAC addresses.
  - PBB-TE/PBT/PBB tags.
  - (T)MPLS labels.
  - Any combination of L2/3/4 headers.
  - VC/VP identifiers.
- Highly optimized memory interfaces to low cost commodity SRAM/SDRAM.
- No Content Addressable Memory (CAM) required.

Figure 1 Overview

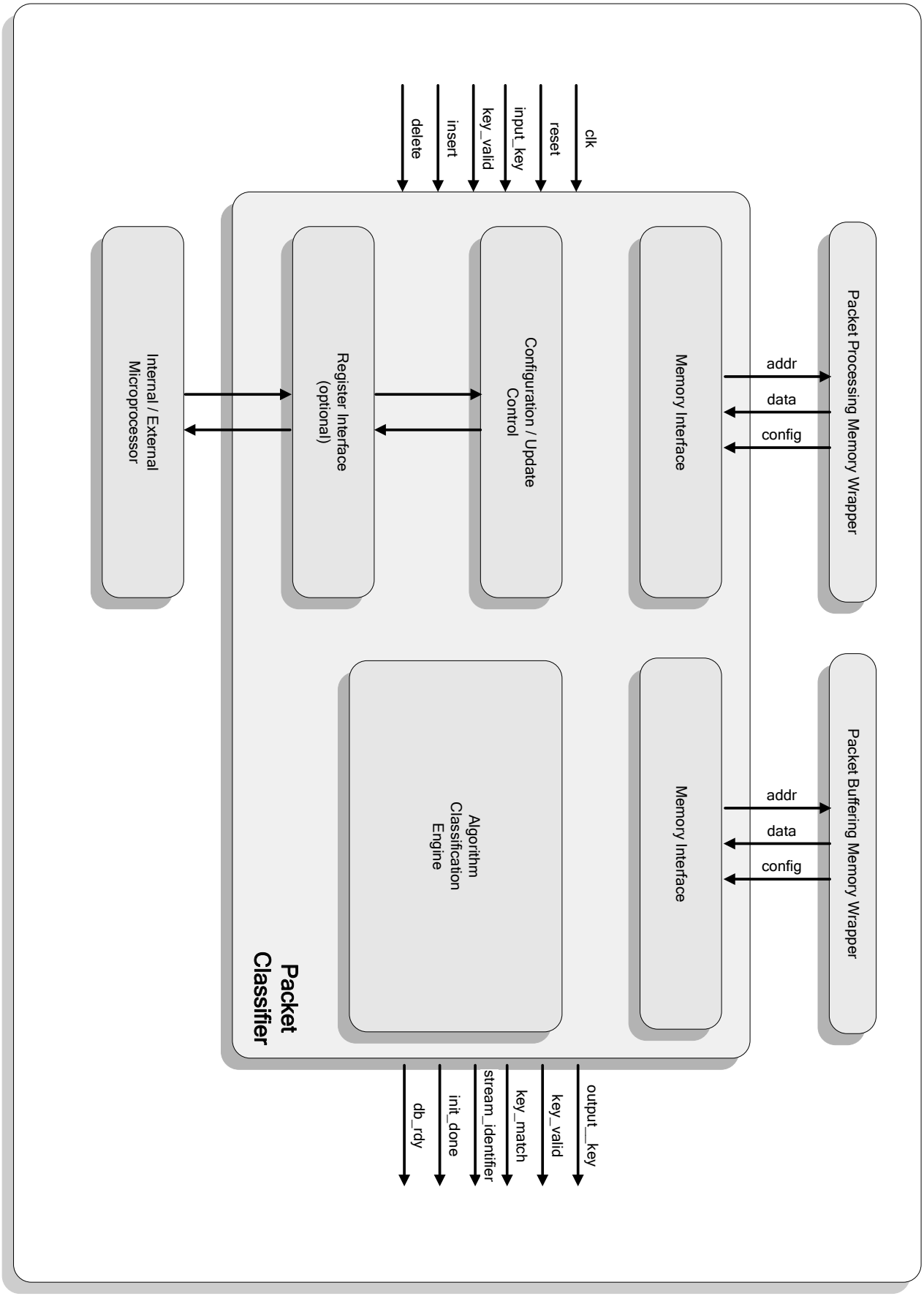
The Packet Classifier shown in figure 1 below is a high performance pipelined and fully synchronous core with standard interfaces to generic memory devices. No specialist network processor or TCAM support is required. The input key presented to the core is compared against a high density search database using a proprietary algorithmic classification engine, and the result of the lookup returned together with any stream identifier associated with the match.

The memory interface parameters to the Packet Processing Memory and Packet Buffering Memory are dependent on the preferred memory technology. The core supports flexible memory interfaces to any generic RAM technology. RAM requirements are determined by the required database capacity and throughput performance. Fast, hitless update of the search engine database is available through a simple register interface.

The core performs the following high level functions.

- Start Up & Database Initialization.
- Key Insertion & Learning.
- Key Deletion and Unlearning.
- Key Lookup.
- Key Lookup with in-band insertion.
- Key Lookup with in-band Deletion.

Figure 1: Architectural Block Diagram



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Protocol, OAM & QoS Support

Multi-Protocol Support.

- OTN (ITU-G.709).
- SONET/SDH.
- MEF E-Line, E-LAN and E-Tree support.
- PBB/TE support - (IEEE801.1ah/Qay/ad).
- (T)MPLS (ITU-T G.81xx).
- VPLS.
- Pseudowire Emulation (PWE3).
- Ethernet/MPLS Multicast.
- Multi-channel TDM Packet Mapping.
- IPv4/IPv6 Classification.

Advanced OAM Support.

- Ethernet OAM PDU support.
- MPLS OAM PDU support.
- Carrier Class Protection Switching.
- Fully configurable OAM snooping and filtering.
- Fully configurable performance monitoring.
- Fully configurable alarm reporting.

Advanced QoS Support

- 256k flows with multiple classes per flow.
- Configurable single or dual bucket policing.
- Fully configurable hierarchical scheduler.
- WFQ, WRR, WRED and strict priority-based scheduling.
- MEF compliant policing.

Target Families & Deliverables

Altera

- Stratix, Arria, Cyclone.

Xilinx

- Virtex, Kintex, Artix.

IP

- EDIF/BIT/SOF/QSF/UCF. Encrypted ModelSim & Back annotated VHDL

Documentation

- Datasheet, Verification Results, User Guide.

Contact Us

info@aliathon.com

+44 (0)1383 737 736

www.aliathon.com

Aliathon Ltd

Evans Business Center, Pitreavie Court

Dunfermline, Fife, KY11 8UU

Scotland, UK

Alliances