Specialist FPGA solutions for OTN, SONET/SDH and PDH networks
About Aliathon
Why Aliathon?
Markets
Products
Partners
Contact Details.
Our Vision...
We are an self funded, sustainable and profitable organization. We deliver well packaged, efficient and cost effective FPGA solutions to network equipment manufacturers.

We achieve this by:
• Acting and delivering like the most flexible silicon solution on the planet.
• Working hand in hand with our clients to develop long term equitable partnerships instead of 1-off financial transactions.

Our people are motivated self starters who learn from & drive each other. In other words we don’t carry passengers... We thrive on the challenges that our business presents, take pride in our work and make sure we enjoy the journey.
Quick Facts….

- 65+ combined years of complex systems and FPGA market experience.
- In-Depth Knowledge of Communications Standards.
- Market segment driven solutions portfolio.
- Ongoing Research Program.
  - Packet & Network Convergence
Clients....

- Ranging from global telecommunications market makers to niche and bespoke communication solution providers.

Markets....

- Aliathon operate across 5 main market segments;
  - Communications
  - Network Analytics / Service Assurance
  - Military
  - Test & Measurement
  - Video Networking
Solutions....

- We develop innovative FPGA based solutions to help our customers process, terminate, generate, inspect, multiplex and attenuate every frame or packet carried through their OTN, SONET/SDH & PDH networks.
- We blend our TDM framing, mapping and packet solutions with your unique systems requirements to deliver the perfect fit for your project needs.
Technical / Commercial Flexibility.....

- Partnership business model designed to share risk & rewards.
- Professional support through entire product lifecycle.
- Perfect Fit - Only pay for what you want.
- Obsolescence proof
- FPGA Architecture expertise.
- FPGA Vendor independent.
Design Expertise.....

- **Strong Software Design Background.**
  - Highly Abstracted Design approach.
- **Expert VHDL language knowledge.**
  - HDL -> Gates...
  - Resource shared but functional coupling avoided...
  - Test & Verification (coverage & reuse).

```vhdl
-- pipeline for re-configure outputs
begin
  if reset then
    pdh_col_pl <= std_logic_vector(others => '0');
    pih_col_pl <= std_logic_vector(others => '0');
  end if;
end process;
```

Why Aliathon?
Why Aliathon?

Our Business Model

NRE

Run Time License

Extended Support

Typical Project Plan

Architecture Decision
- FPGA Vs. ASIC ASSP

Project Design Phase
- FPGA Architecture Definition & Design

Field Trial & Volume Production
- Software And IP Integration

- ECO Changes

Product Support
- Hardware, Firmware, Software Iteration
- Bug Fixes
- Additional Market Requirements
Guaranteed Support when you need it most....

- Continue to reply on Aliathon’s expertise, freeing up your team to concentrate on other tasks.
- Ensure longevity of support from Aliathon.
- Critical & Non-Critical Fault resolution.
- 200 hours direct access to solutions designers + 3 days on-site training.
- IP ports to different FPGA families, vendors and tools releases.
- Respond quicker to market/customer requirements.
## Support Options

<table>
<thead>
<tr>
<th>Support Packages</th>
<th>Basic Support</th>
<th>Priority Telephone Support</th>
<th>Priority Email Support</th>
<th>Auto Updates</th>
<th>Cost</th>
<th>Support Contract Length</th>
<th>Support Scope</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Free</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bronze</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>15% project cost</td>
<td>6 months</td>
<td>Project</td>
</tr>
<tr>
<td>Silver</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>20% project cost</td>
<td>12 months</td>
<td>Project</td>
</tr>
<tr>
<td>Gold</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>30% project cost</td>
<td>24 months</td>
<td>Project</td>
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<tr>
<td>Corporate</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Negotiable</td>
<td>Negotiable</td>
<td>Site/Global</td>
</tr>
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</table>
Our Markets
<table>
<thead>
<tr>
<th>Communications</th>
<th>Test &amp; Measurement</th>
<th>Network Analytics / Assurance</th>
<th>Military</th>
<th>Video Networking</th>
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</thead>
<tbody>
<tr>
<td>Mobile Backhaul (MBH)</td>
<td>Fibre-Optic Installation &amp; Maintenance</td>
<td>Traffic Analysers / Monitors</td>
<td>Custom Comms Networks</td>
<td>Video / Data Network Interface Cards</td>
</tr>
<tr>
<td>Multi-Service Metro (MSPP, MSAN, ADM)</td>
<td>Bit-Error rate (BERT) Products</td>
<td>Intrusion Detection Systems</td>
<td>Global Information Grid (GIG) analytics</td>
<td>Optical Interfaces / Converters</td>
</tr>
<tr>
<td>Data Centre Interconnect / Datacom Networks Transport</td>
<td>Data Generators &amp; Analysers</td>
<td>Cyber Security &amp; Content Security Gateways</td>
<td></td>
<td></td>
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<tr>
<td>40G/100G Transport / Transmission (LH DWDM)</td>
<td></td>
<td>Information Assurance</td>
<td></td>
<td></td>
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</table>
Architectural Examples: Comms

Transponder

(Termination & Mapping at similar line rates, e.g. 100<>100, 40<>40 etc).

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<tr>
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<th>Line Rates</th>
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<tbody>
<tr>
<td>OTN</td>
<td>SONET/SDH</td>
</tr>
<tr>
<td>OTU4</td>
<td>OC768/STM256</td>
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<tr>
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<td>OC12/STM4</td>
</tr>
<tr>
<td></td>
<td>OC3/STM1</td>
</tr>
<tr>
<td>Packet</td>
<td></td>
</tr>
<tr>
<td>10/40/100 GE</td>
<td></td>
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Architectural Examples : Comms

Muxponder

(muaxing of lower rate signals into higher rate carrier)

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<tr>
<td>PDH</td>
<td>E1/T1</td>
</tr>
<tr>
<td></td>
<td>E3/T3</td>
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<tr>
<td>Cell/Packet</td>
<td>1/10/40/100 GE</td>
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<tr>
<td></td>
<td>FC</td>
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<tr>
<td></td>
<td>PoS</td>
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<tr>
<td></td>
<td>HDLC</td>
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<tr>
<td></td>
<td>ATM</td>
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Architectural Examples: Comms

Add-Drop MUX

(add/drop of lower rate signals from higher rate carrier)

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ADM Rates

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PDH
- E1/T1
- E3/T3

Cell/Packet
- 1/10/40 GE
- FC
- PoS
- HDLC
- ATM
Architectural Examples: Comms

Repeater / Regenerator

(termination and re-transmit using same payload structure)

Client Rates
- OTN
- OTU4: OC768/STM256
- OTU3: OC192/STM64
- OTU2: OC48/STM16
- OTU1: OC12/STM4
  OC3/STM1

Line Rates
- OTN
- OTU4: OC768/STM256
- OTU3: OC192/STM64
- OTU2: OC48/STM16
- OTU1: OC12/STM4
  OC3/STM1
Our Solutions
OTN Network Interface

--- Edge / Access ---
--- Metro ---
--- Core ---

FEC → OTN Framer → SONET/SDH Buffer → Multi-Port SDH Digital Wrapper

FEC → ODUx MUX → ODUx Mapper → Multi-Port OTN Mapper / Retimer

FEC → ODUx MUX → OTN Framer → Multi-Port OTN Aggregator

FEC → GFP-F Framer → GFP-T CODEC → Packet-OTN Transport

Client Side Interface
SONET/SDH
OTN
Packet
Video
OTN Framer
- Supports OTU1-OTU4 line rates
- Conforms to G.709.
- G.709 FEC (GFEC) and optional EFEC support
- Processes OTUk, ODUk and OPUk overhead
- Supports synchronous (ATM, GFP) and asynchronous (SONET/SDH) payload mapping (accommodating positive/negative stuffing).

ODU Mux
- Supports G.708 Muxing of client ODU0/1/2/3 signals into ODU1/2/3/4
- Full OTN overhead processing for intermediate stages
- 1 and 2 stage mux/demux functionality.

GFP-F (Framer)
- Compliant with ITU-T G.7041 specification.
- Generates/Synchronises to GFP data stream including IDLE frames.
- Provides GFP scrambling/descrambling.
- Full Overhead and Defect processing

GFP-T CODEC
- Compliant with ITU-T G.7041 specification.
- Encodes input blocks into 67 byte GFP-T blocks as per G.7041.
- Extracts 64 byte 8B/10B blocks of data from GFP-T frames.
Products: SONET/SDH

SONET/SDH Network Interface
--- Edge / Access ---
--- Metro ---
--- Core ---

Client Side Interface
SONET/SDH
PDH
Packet Video

Next Gen Packet-over-SONET
Traditional Packet-over-SONET
HD Channelized Cell
LO Channelized Cell
Native Channelized TDM
Circuit Emulation
LO Channelized HDLC
SONET/SDH Framer
- Support for OC3/STM1, OC12/STM4, OC48/STM16, OC192/STM64 and OC768/STM256
- Single & multiple line interface support
- Conforms to G.707, G.806, G.783 and T1.105.
- Processes all STS/AU pointers and Higher Order paths.
- Full Overhead and Defect processing for all line interfaces and STS/VC paths

VT/TU Mapper
- Conforms to ITU G.707/ANSI T1.105
- Maps/Demaps multiple Lower Order VT/TU paths.
- All permutations of mapping path and VT/TU type supported
- Generates/Processes all VT/TU pointers.
- Full Lower Order Path Overhead processing

E1/T1 Mapper/Framer
- Framing and deframing for up to 1008/1344 E1/T1 channels (enough for a full OC48/STM16).
- Asynchronous and synchronous TU payload mapping/demapping
- Conforms to ITU G.704/ANSI T1.403.
- Frame generation and synchronization for T1, J1 and E1 PDH signals.
- Full Overhead and Defect processing per channel.
- Channel frame formats may be configured dynamically and independently, and asynchronous channel timing is supported.
E3/T3 Mapper/Framer
- Performs frame synchronization and generation for T3, J3 and E3 PDH signals.
- Asynchronous and synchronous STS1/VC3 payload mapping/demapping
- Conforms to ITU G.704/ANSI T1.403.
- Core is capable of framing and deframing up to 24 channels (enough for a full 2 x OC12/STM4).
- Full Overhead and Defect processing per channel.
- Channel frame formats may be configured dynamically and independently, and asynchronous channel timing is supported.

POS Framer
- Supports OC3/STM1 through to OC192/STM64.
- Designed to process concatenated SONET/SDH payloads.
- Support for CRC-16 and CRC-32.

ATM Framer
- Conforms to ITU I.432.1.
- Processes data for multiple independent TDM ATM streams.
- Configurable IDLE and Unassigned Cell insertion, detection and deletion.
- Optional HEC insertion; HEC error detection and correction.

HDLC Framer
- Multi-channel HDLC support (>8k channels)
- Supports bit-synchronous and byte-synchronous HDLC.
- Configuration may be applied to each stream independently, and changed dynamically.
- Full Overhead and Defect processing per channel
E1/T1 LIU/Framer
• Conforms to ITU G.704/ANSI T1.403.
• Performs frame synchronization and generation for T1, J1 and E1 PDH signals.
• Serial clk+data line interface support for connecting to standard E1/T1 LIUs.
• Jitter attenuation for up to 504/672 E1/T1 channels (2xOC12/STM4 links).
• Designed to provide G.832 and G.824 Output Jitter Compliance, for 2.048 kHz +/-50 ppm (E1), 1.544 kHz +/-32 ppm (T1).

E3/T3 LIU/Framer
• Conforms to ITU G.704/ANSI T1.403.
• Generates and performs frame synchronization for T3, J3 and E3 PDH signals.
• Supports up to 24 serial clk+data E3/T3 line interfaces
• M13 (DS3->DS2-DS1) and E3->E2->E1 support.
POS Framer
• Supports OC3/STM1 through to OC192/STM192.
• Designed to process concatenated SONET/SDH payloads.
• Inserts and detects CRC-16 and CRC-32.

ATM Framer
• Conforms to ITU I.432.1.
• Processes data for multiple independent TDM ATM streams.
• Configurable IDLE and Unassigned Cell insertion, detection and deletion.
• Optional HEC insertion; HEC error detection and correction.

HDLC Framer
• Multi-channel HDLC support (>8k channels)
• Supports bit-synchronous and byte-synchronous HDLC.
• Configuration may be applied to each stream independently, and changed dynamically.
• Full Overhead and Defect processing per channel.
GFP-F (Framer)
• Compliant with ITU-T G.7041 specification.
• Generates/Synchronises to GFP data stream including IDLE frames.
• Provides GFP scrambling/descrambling.
• Full Overhead and Defect processing

Ethernet MAC
• Tri-rate (10/100/1000) & 10Gb Ethernet support. Compliant to IEEE-1588
• CRC-32 checking & generation
• Programmable frame length to support proprietary and standard frame lengths.
• Network statistics.
Our Partnerships