

## Why Our Clients Choose Us....

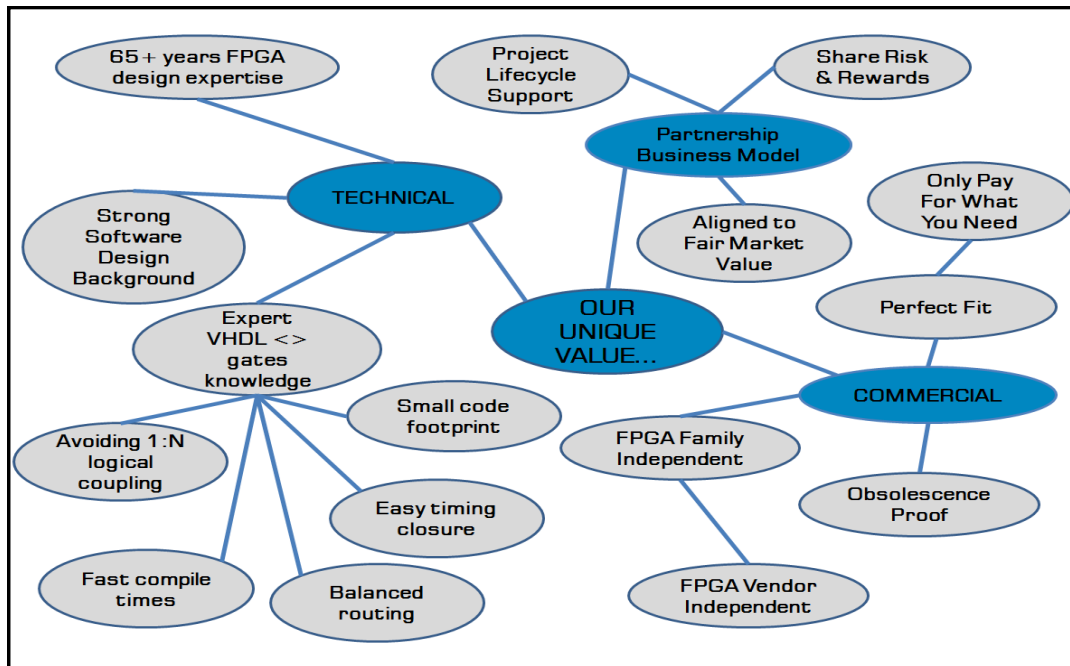
We are a well established, trusted and highly experienced team of FPGA solutions providers. Our target markets are Communications, Network Analytics & Assurance, Military, Test & Measurement and Video Networking.

Since 2001 we have been providing our clients with the ability to process, terminate, generate, inspect, multiplex and attenuate every packet or frame running through their products.

Aliathon's solutions live at the core of 100's of active client designs shipping in 100,000's of products today.

Aliathon have been a member of the Altera & Xilinx partnerships since 2004 and have experience of delivering our solutions across all mainstream families from both companies.

**We know that our unique value makes us stand out from the crowd..... we can help to make your products do the same.....**



## Market & Application Focus.

### Communications

1. Mobile Backhaul (MBH).
2. Multi-Service Metro (MSPP, MSAN, ADM).
3. Data Center Interconnect / Datacom Network Transport
4. Transport/ Transmission (LH DWDM).

### Network Analytics & Assurance

1. Traffic Analyzers / Monitors.
2. Intrusion Detection Systems.
3. Cyber & Content Security Gateways.
4. Information & Service Assurance

### Military

1. Custom Communications Networks.
2. Global Information Grid Analytics (Collecting, Processing, Analyzing, Disseminating).

### Test & Measurement

1. Fiber-Optic Installation & Maintenance.
2. Bit-Error Rate (BERT) Products.
3. Data Generator & Analyzers.

### Video Networking

1. Video / Data Network Interface Cards.
2. Optical Interfaces / Converters

## Optical Transport Network

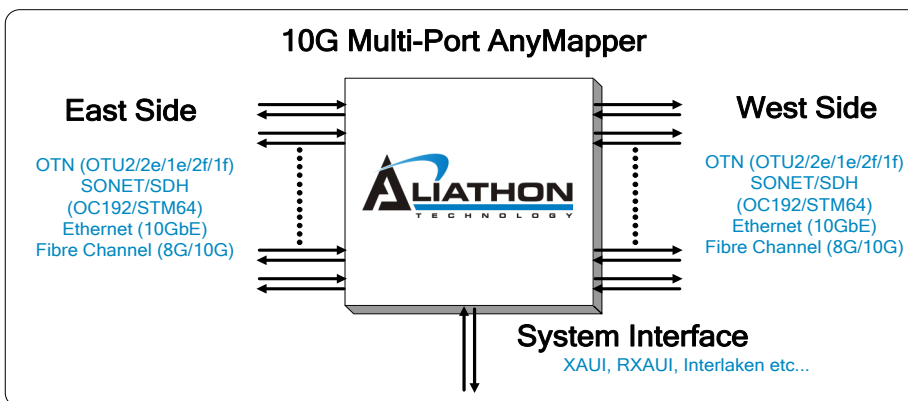
Aliathon's OTN solutions are targeted towards TDM line side connectivity & TDM/packet transport across the communication network (access/edge, metro & core/transport). All cores are fully compliant with the G.709 ITU-T standard. Each design is offered in BIDIR and Rx-only modes.

We support rates from 1Gb-100Gb (OTU1-OTU4) in single & multi-port configurations. The fine-grained flexibility supports all types of TDM & packet protocol natively and mapped in to in the OTUk. Encapsulation schemes supported are GMP, BMP & AMP.

The OTN framer technology provides forward error correction options for both G.709 RS FEC (2.5G 10G & 100G) and G.975.1 eFEC (10G). Proprietary schemes such as CI-BCH for longer optical reach can also be provided.

Errors, defects & statistics are provided for all layers via a fully customizable  $\mu$ Processor interface.

### Example Architectures



#### Key Features

Rich array of client signals & mapping styles.

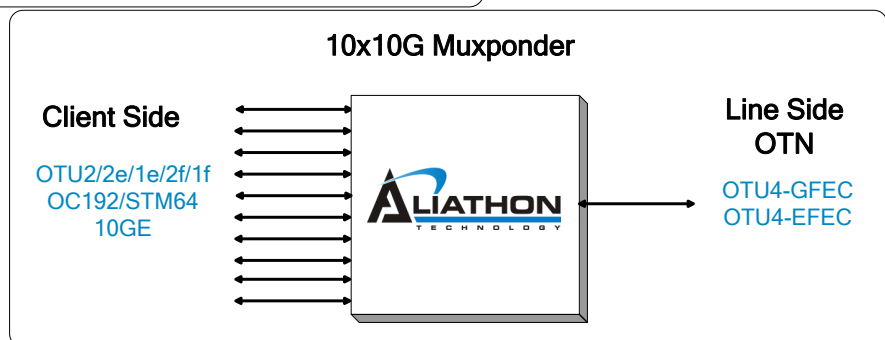
Flexible packet interface allowing transmission convergence between TDM & packet worlds.

Supporting a range of line & system interfaces enabling connectivity to any optical module or backplane architecture.

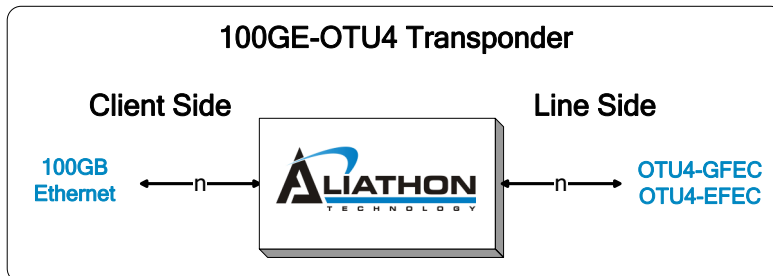
#### Key Features

Rich array of client signals & mapping styles.

Line side GFEC & optional CI-BCH eFEC for long reach applications.



### 100GE-OTU4 Transponder



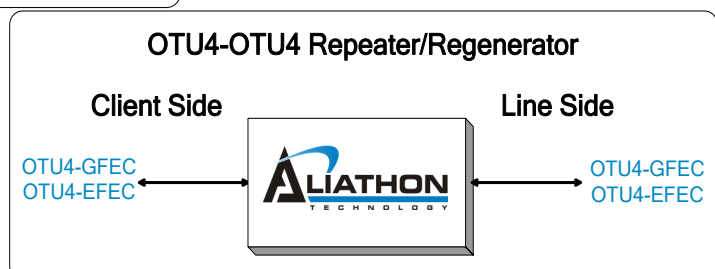
#### Key Features

Fully support for Ethernet stats in the ingress & egress directions.

Line side GFEC & optional CI-BCH eFEC for long reach applications.

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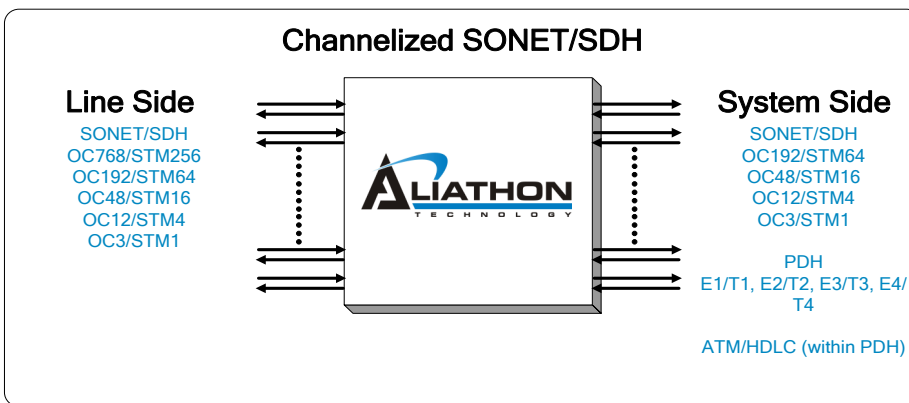
## SONET/SDH

Aliathon's SONET/SDH solutions are targeted towards TDM line side connectivity & TDM/packet transport across the communication network (access/edge, metro & core/transport). All cores are fully compliant with the G.707, G.806, G.793 & T1.105 ITU-T standard. Each design is offered in BIDIR and Rx-only modes.

We support rates from 155M (OC3/STM1) to 40G (OC768/STM256) in single & multi-port configurations. The fine-grained flexibility supports all types of TDM & packet protocol natively and mapped in to in the payload via any of the VT/TU paths. Encapsulation schemes supported channelized TDM (sub rate SONET/SDH & PDH signals) and concatenated for packet (GFP, PoS/HDLC, ATM,).

Errors, defects & statistics are provided for all layers via a fully customizable  $\mu$ Processor interface.

### Example Architectures



#### Key Features

High bandwidth / deeply channelized cores supporting all line rates and mapping paths.

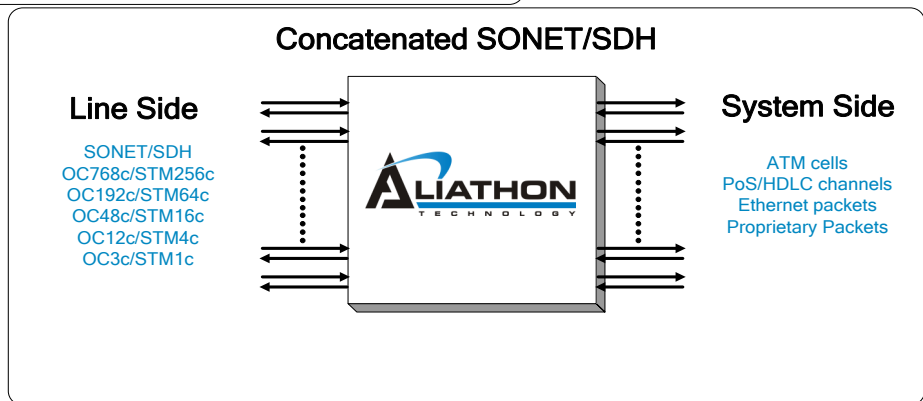
Full high & low order path processing including all PDH tributary time-slots.

#### Key Features

High bandwidth / deeply channelized cores supporting all line rates and mapping paths.

Supports all common concatenated types including ATM, PoS (HDLC) and Ethernet.

Can be configured to support any proprietary packet type.

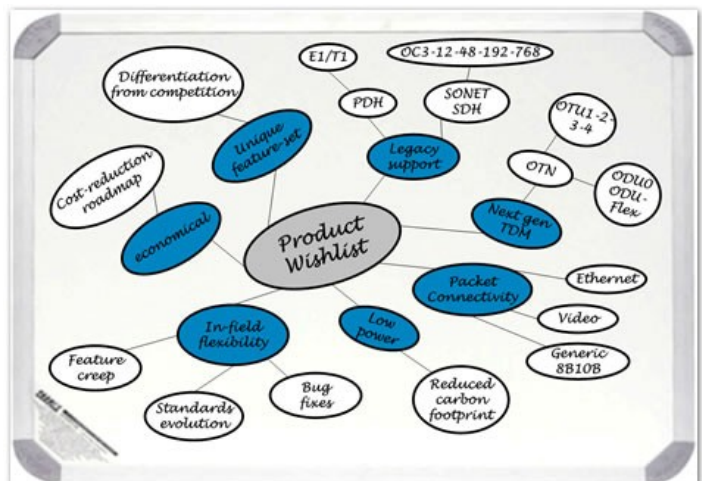


## Customization

Here at Aliathon we understand that differentiating from the competition is important to you. You don't want to design products that look, feel and perform the same as everyone else's.

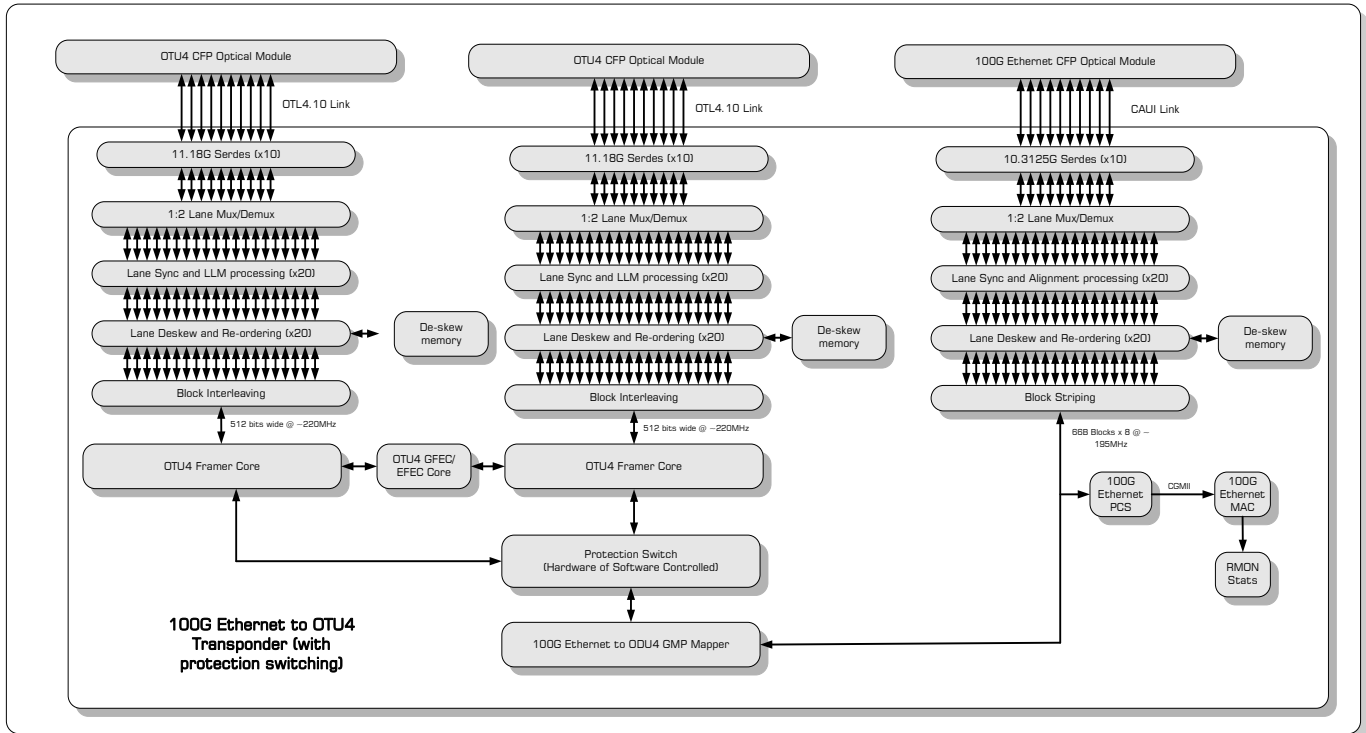
We blend our TDM & packet building blocks with your unique requirements to give you the perfect fit for your project needs.

All project specific design blocks are delivered to you as clearly commented HDL code that are 100% owned by you.



## Packet / Cell Solutions...

### Application Case Study : 100GE-OTU4 Transponder w/protection.



The diagram above represents an example of Aliathon's capabilities in the optical transmission domain.

This design has 2 identical OTU4 paths. The OTU4 path implements an OTL4.10 interface. This incorporates 10 11.18G SERDES, bit demuxing (to translate to an OTL4.20 interface) and individual lane framing, based on the OTU4 FAS pattern and the inserted LLM bytes. The individual lanes are deskewed and re-order to reconstitute the OTU4 signal. The OTU4 core provides standard G.709 OTN framing and processing, based on a 512-bit bus in this case. Overhead processing and standard G.709 FEC (GFEC) or EFEC are provided. Each of the OTU4 signal paths interfaces to a simple protection switch (bridge & switching functions) under the control of an external micro processor or an internal hardware trigger (to indicate lost of frame or a specified error rate).

On the Ethernet side, 10 10.3125G SERDES are used to implement a CAUI interface. After bit de-muxing, the individual lanes are 66B de-framed, de-skewed and reorder to produce an interface that is 8 aligned, contiguous 66B codewords wide. This interface connects to the 100G Ethernet to OTU4 mapping block. Passive Ethernet RMON monitoring is provided with a PCS block to provide 66B decoding, and a 100G Ethernet MAC for frame delineation and CRC error detection. The 100G Ethernet to OTU4 mapper blocks maps the 66B codewords into an ODU4 payload for transport by the OTU4 framer.

**Design Size : 220K LUTs—280K LUTs (GFEC/EFEC dependant). Standard Transponder (without protection) 160K LUTs—220K LUTs (GFEC/EFEC dependant).**

#### Summary

In this instance our client needed to solve a transponder problem that could not be efficiently implemented in any off-the-shelf ASSP\* solution.

The combination of Aliathon's unique solution (logic/memory consumption, resource sharing/efficiency, risk-sharing business model) and today's cost effective and powerful FPGA fabrics (logic/memory density, transceiver count etc) allows the delivery of a solution that beats the ASSP\* offering in cost, power consumption, features and flexibility.

Further cost saving are realized at the project level in areas such as reduced chip count (reliability, test/verification complexity) and a simplified software layer.

Lastly the client can continue to generate additional revenues through the reconfigurable nature of the FPGA and the scalable & modular approach of the Aliathon solution, neither of which would have been available from the ASSP\* device.

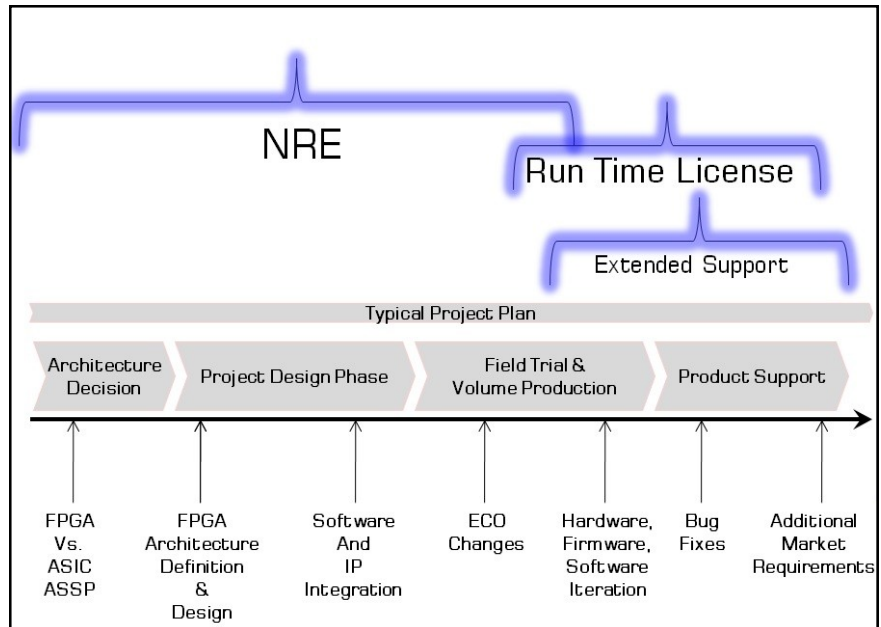
\*Application Specific Standard Product.

## Business Model

Our business model is designed to support your project from early concept all the way through to production and beyond (including in-field upgrades).

We offer a commercially compelling alternative to fixed-function products and other IP providers.

We give you cost, power and real-estate savings while at the same time delivering the flexibility & reliability that your products need.



## Contact Us.....



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## Alliances.....

